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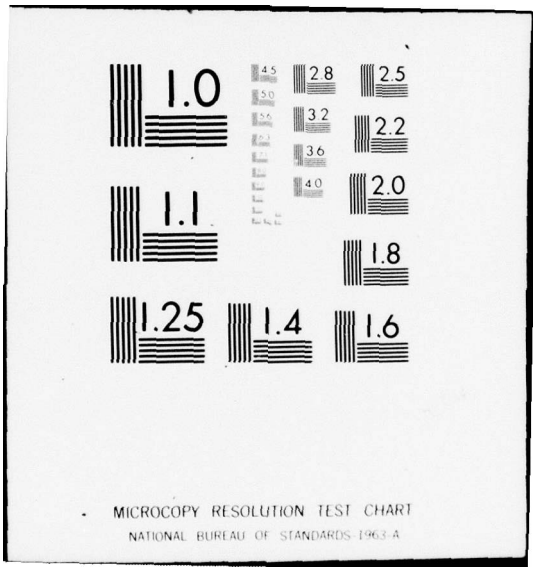
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DEVELOPMENT OF A LINEAR OCTAVE-BANDWIDTH 2- TO 4-GHz TRANSISTOR AMPLIFIER

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RCA Corporation
David Sarnoff Research Center
Princeton, NJ 08540

TECHNICAL REPORT AFAL-TR-75-127

AUGUST 1975

FINAL REPORT for the Period
15 March 1973 to 14 March 1975

Prepared for

AIR FORCE AVIONICS LABORATORY
Air Force Wright Aeronautical Laboratories
Air Force Systems Command
Wright-Patterson Air Force Base, Ohio 45433

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This technical report has been reviewed and is approved for publication.

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Chief, Signal Reception and Control Group
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FOR THE COMMANDER:
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Acting Director
Electronic Technology Division

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C_{ob} reduction
Gold metallization
Large-signal S-parameter measurements

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The objective of this program was to develop a linear power transistor capable of delivering 5 W of linear output power in the 2- to 4-GHz frequency range with a minimum gain of 10 dB and an efficiency of 10%. The transistors developed on this program were performance-tested to characterize their parameters for broadband capability. This information was then used to design a single and a dual transistor circuit to demonstrate broadband performances from 3.4 to 4.0 GHz.

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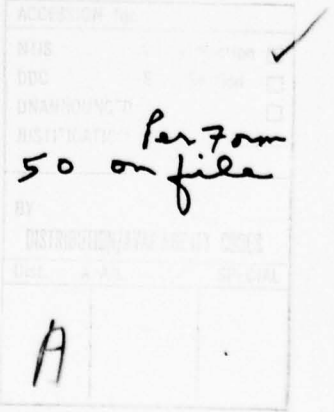
During the course of this program, a new state-of-the-art device, RCA type TA8791, was designed to achieve linear operation with high output power at 4 GHz. Because a large number of transistor cells (16 cell-pairs) were required to obtain a linear output power of 5 W, the final device consists of two separate 8 cell-pair transistors paralleled directly in the microwave circuit.

A number of process improvements were implemented; the most successful of them were the ion implantation, the double-epitaxial layer, and the ultra-thin pellets with integral heat spreaders. All final devices featured emitter-site ballasting optimized for best rf output power together with good linearity and acceptable sharing of the dc bias current between the various transistor cells. The transistor pellets were mounted on microstrip BeO carriers. These carriers feature low thermal resistance, low electrical parasitic elements, and integral input and output rf tuning for low rf losses and best operating bandwidth.

A unique computer-controlled infrared microscope was used to analyze the temperature of the transistor pellets mounted on the microstrip carriers. Also, computer-controlled measurement equipment greatly aided in the characterization of the rf parameters of the transistors. Based on this information, the rf circuits were designed and optimized over the desired frequency band by an optimum-seeking computer program.

Two broadband amplifiers were developed: one utilizing a single transistor (8 cell-pairs) and a second one utilizing two transistors (16 cell-pairs in total) paralleled directly in the microstrip circuit. Best broadband performance was obtained with the single transistor amplifier, which delivered 2.5 W of output power with an input power of 0.4 W in the frequency range from 3.4 to 3.8 GHz and a small-signal gain of about 9 dB.



PREFACE

This Final Technical Report describes work performed by members of the Technical Staff of RCA's Solid State Division at Somerville, NJ, and of the Microwave Technology Center at Princeton, NJ, under Air Force Contract No. F33615-73-C-1118, Project No. 69CK, Task No. 01 28. The contract was administered under the technical direction of Mr. N. DiGiacomo, AFAL/DHM, of the Avionics Laboratory, Wright-Patterson Air Force Base, Ohio.

This report summarizes the work effort under the entire contract period with emphasis on the last six months. Readers wishing to obtain data on the first 18 months are referred to the previously issued technical reports [1-3].

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1. R. Duclos and A. Presser, "Development of a Linear Octave-Bandwidth 2- to 4-GHz Transistor Amplifier," Technical Report AFAL-TR-74-7, prepared for Air Force Avionics Laboratory under Contract No. F33615-73-C-1118, June 1974.
2. R. Duclos, "Development of a Linear Octave-Bandwidth 2- to 4-GHz Transistor Amplifier," Technical Report AFAL-TR-74-267, prepared for Air Force Avionics Laboratory under Contract No. F33615-73-C-1118, October 1974.
3. R. Duclos and F. Sechi, "Development of a Linear Octave-Bandwidth 2- to 4-GHz Transistor Amplifier," Technical Report AFAL-TR-74-347 prepared for Air Force Avionics Laboratory under Contract No. F33615-73-C-1118, February 1975.

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SECTION I

INTRODUCTION

The objective of this program, as stated in the contract and modified in October 1974, was the development of a high-power bipolar transistor capable of delivering 5 W of linear output power in the 2- to 4-GHz frequency range.

The program was divided in two phases: device development and amplifier development. The device development consisted of the design of the transistor pellets, the design of large microstrip carriers, and the rf evaluation of all the devices that were fabricated. The amplifier development consisted of the design and rf evaluation of broadband amplifiers. The design and the fabrication of the transistor pellets were performed in the RF and Microwave Devices Department, RCA Solid State, Somerville, NJ, while the rf evaluations, the development of the plated heatsink technology, and the design of the microstrip carriers and of the broadband amplifiers were performed at the Microwave Technology Center, RCA Laboratories, Princeton, NJ.

A first transistor design, RCA type TA8870, was used for the evaluation of many processes. It was then followed by the TA8791 which is considered to be the final design. The TA8791, when compared with the TA8870, has better high-frequency performance and better thermal characteristics. A number of special processes were evaluated for the fabrication of these transistors: metal-grid overlay, epitaxial-base selective oxidation, ion implantation, double-epitaxial layer, ultra-thin pellets with plated heatsink, and combination of emitter-site and finger ballasting. Only the ion implantation, the double-epitaxial layer, and the ultra-thin pellets with plated heatsink were successful and were used in the final design.

A transistor able to provide 5 W at 4 GHz required 16 cell-pairs. This large size causes very low fabrication yield and low power-combining efficiency; therefore, the final device was fabricated with two separate 8-cell-pair transistors paralleled directly on the microwave circuit. Two broadband amplifiers were designed, a first one operating with a single 8-cell-pair device and a second one operating with two of these devices in parallel.

As required by this program, the two broadband amplifiers and a total of 12 transistor samples were delivered.

SECTION II

POWER TRANSISTOR DEVELOPMENT

A. TRANSISTOR DESIGN

1. Design of the TA8791

The transistor design to meet the 5-W linear power-output performance at 2 to 4 GHz utilizes 16 cell-pairs of the multiple-base-cell structure shown in Fig. 1. In order to obtain a reasonably high yield, 8 cell-pair transistors were fabricated, selected in pairs, and paralleled directly in the microwave circuit. The basic cell design for this transistor is a heavily emitter-ballasted overlay structure which is based upon scaling from the RCA TA8870 transistor design. In this new design, particular consideration has been given to the metallization fingers to optimize the efficiency of the input circuit. Specifically, the emitter- and base-finger lengths have been shortened, and the base fingers have been widened relative to the RCA TA8870. In

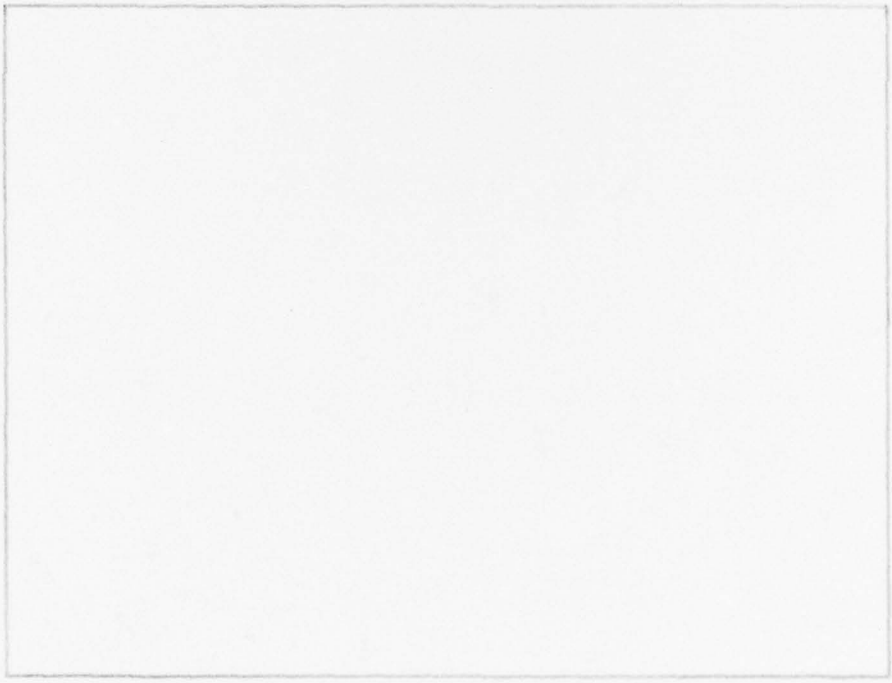

Figure 1. RCA TA8791 transistor (single-cell pair).

this way, the frequency-dependent impedance of these fingers has been reduced to improve power gain and input-circuit efficiency. To reduce the effects of thermal saturation, the size of the base cell (using the emitter periphery criteria) has been optimized so that four cells equal approximately one RCA TA8870 cell. Table 1 shows the design characteristics of the basic two-cell pellet.

Table 1. TA8791 Design Characteristics

Parameter	Value
Base Cells	2
Base Area ($mils^2$)	30.4
Base Periphery (mils)	37.1
Emitter Sites	30
Emitter Area ($mils^2$)	1.26
Emitter Periphery (mils)	86
EDR = EP/BA x I_C/EP (mA/mil^2)	5.68
C_{ob} (pF)	1.43

2. C_{ob} Reduction

In a common-base configuration, the collector-to-base output capacitance (C_{ob}) limits the maximum operating bandwidth of the device. Furthermore, high reactive currents flowing through the common lead connecting the base of the transistor to the electrical ground have a regenerative effect at high operating frequencies with consequent degradation of the transistor linearity. It was therefore decided to modify the TA8791 design in order to reduce the C_{ob} capacitance.

The C_{ob} on the TA8791 is made up of two parts: the junction capacitance and the metal-over-silicon (MOS) capacitance. The junction capacitance is fixed for a given voltage by the geometric design configuration for the device and is not readily reduced. The MOS capacitance is governed by the size of the bonding pads. The TA8791 transistor was first designed for 2-mil-diameter bond wire; however, it was found that there is little difference in the performance when smaller diameter (1.2 mil) bond wires are used. This factor

makes it possible to reduce the bond-pad area and the MOS capacitance. Consequently, a new photomask was designed with a reduced bond-pad area. Figure 2(a) shows the old metal pattern design, and Fig. 2(b) shows the new metal pattern design. There is an overall reduction in C_{ob} of about 20 percent with the new metal pattern.

The wafer run L615 featured this new metallization pattern, and devices from wafer L615-4R have been delivered.

3. Gold Metallization

A new gold-metallization system has been developed under an RCA program and is being applied to the TA8791. Besides showing improved reliability, the advantages of gold metallization are as follows: thicker layers are achieved; reliability is higher; coverage over oxide steps is improved; and experience with other transistor types shows improved performance due to lower rf losses and improved current-handling capability. It is believed, therefore, that gold metallization contributes to the improved performance that is required by the high operating frequency of the TA8791 transistor.

The gold metallization was implemented on a number of wafers and particularly on wafers L605-6 and L615-4R from which transistors have been delivered.

B. ION IMPLANTATION

1. Ion-Implantation on TA8870 Design

The frequency response of transistors with diffused structures can be improved by reducing the base-junction depth to obtain a more step-like impurity profile as shown in Fig. 3. In this way, the impurity concentration under the emitter is increased so that when voltage is applied to the collector-base junction, the depletion region extending into the base is reduced; this prevents punch-through, and the collector-base breakdown voltage may be sustained with a narrow base width. Also, it permits emitter-current injection to take place further from the emitter edge so that the current density is reduced, minimizing base-widening. Using ion implantation for basic doping provides an improved means of achieving a desired impurity profile. A gaussian-type impurity distribution is obtained with ion implantation, but because the

Figure 2. TA8791 metal patterns.

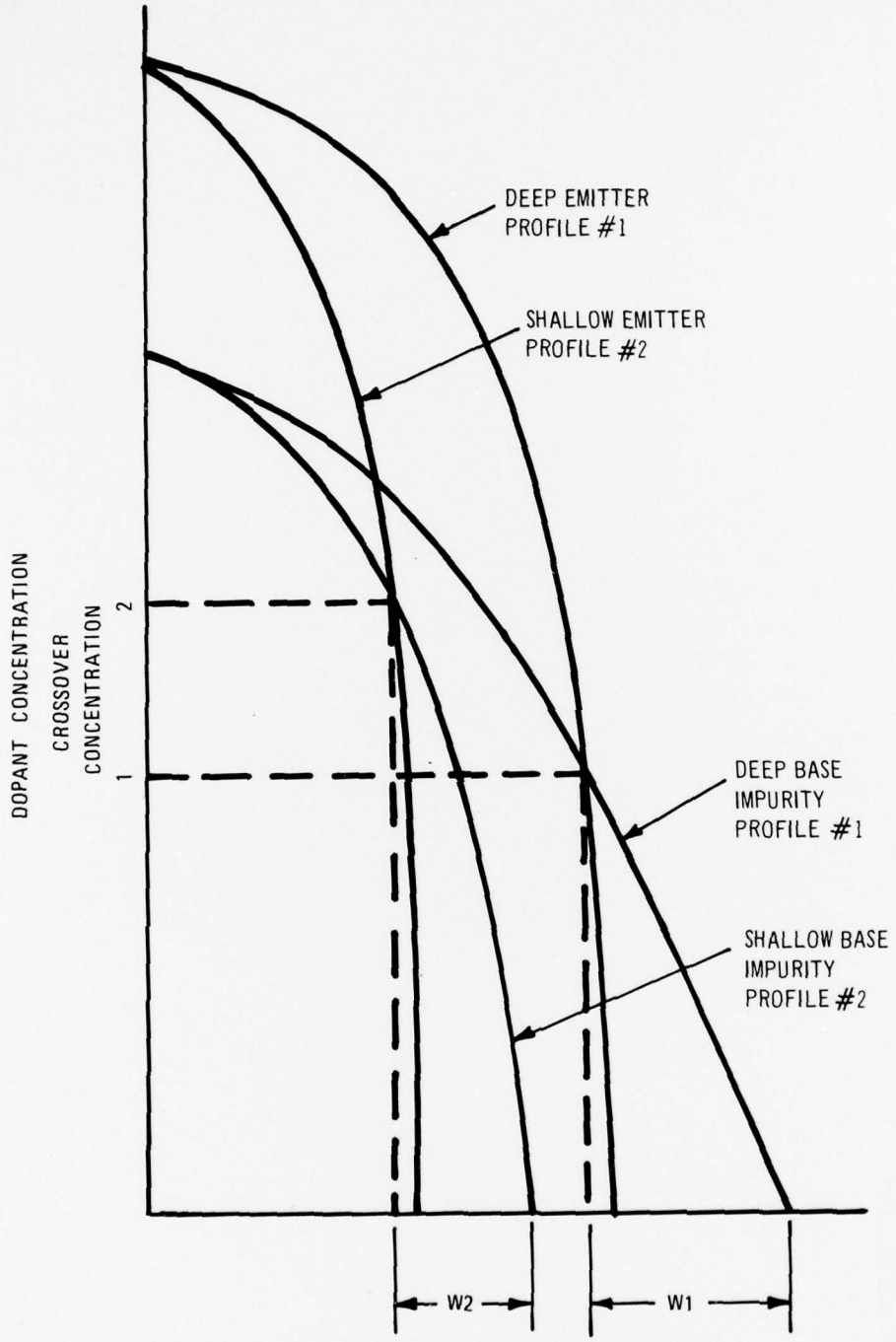

Figure 3. Impurity profiles showing higher impurity concentration with shallow junctions.

ions are energized in an accelerating column and are passed through a beam analyzer which selects out all ions of improper mass and energy, a very uniform beam energy incident on the target wafer is maintained. The wafer is scanned with the ion beam and a digital integrator is used to measure the dose level. The uniform ion energy established by the implanter system means that a tight impurity distribution in the silicon wafer is obtained, and with boron and arsenic implanted atoms, tail-off is slight and sharp front-edge fall-off is achieved, giving a system capable of a very narrow base width.

RCA has two ion-implantation systems; the first system is at the RCA Laboratories in Princeton, NJ. Figure 4 shows a schematic drawing, and Fig. 5 is a photograph of the system. This implanter is essentially two machines in one: a research and development line and a production beam line with a common ion source, accelerating column, and mass separator. Ions can be implanted with one line while work is being set up in the other. RCA's second ion-implantation system is located at the Solid State Technology Center in Somerville, NJ.

A first matrix of experiments, as described in the First Interim Report [1], was started in order to establish the ion-implanted impurity profiles needed for the base region. The experimental vehicle used for this development effort was the TA8870 pellet. Junction depth and peak impurity concentration (N Max) are two important parameters which must be determined in establishing the required impurity profiles for the base and the emitter. Generally, a high impurity concentration is needed in the base-width region of microwave transistors so that high collector-base breakdown voltage can be sustained without punch-through and a low r_{bb}' may be obtained with a narrow base width. But this high doping level must be consistent with adequate emitter efficiency.

From the results, it was clear that the peak impurity concentration of the base-impurity profile should be a minimum of 2.5×10^{19} atoms/cm^3 and that the optimum peak impurity concentration may be even higher.

It was then realized that the existing techniques for n-p junction measurements would not work satisfactorily on ion-implanted profiles, and that an additional effort would be required to develop techniques to evaluate the experimental wafers so that quick and early results of the experiments could be obtained. Without junction-measurement techniques, evaluation could be made

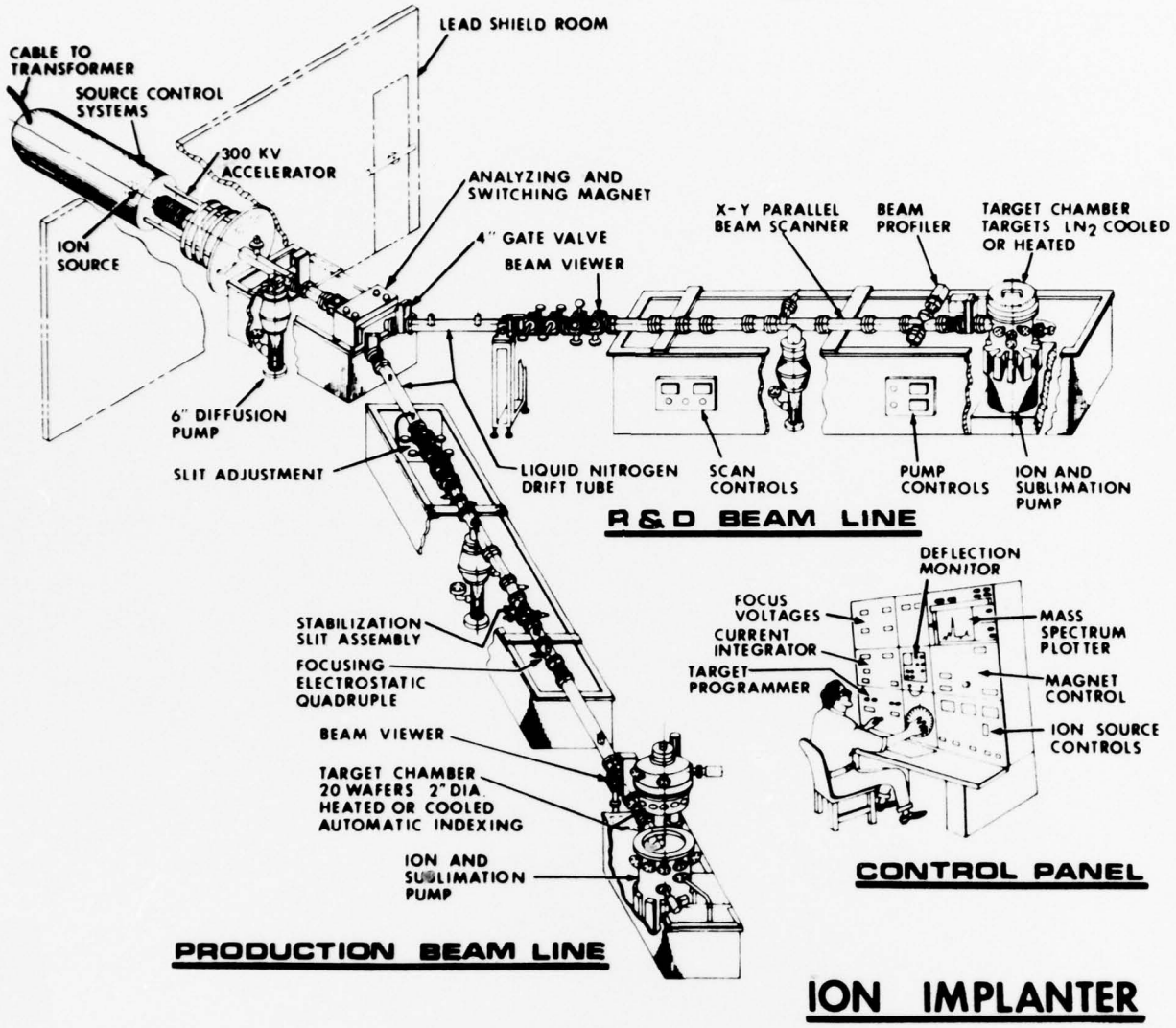

Figure 4. Ion-implantation facility at RCA's David Sarnoff Research Center.

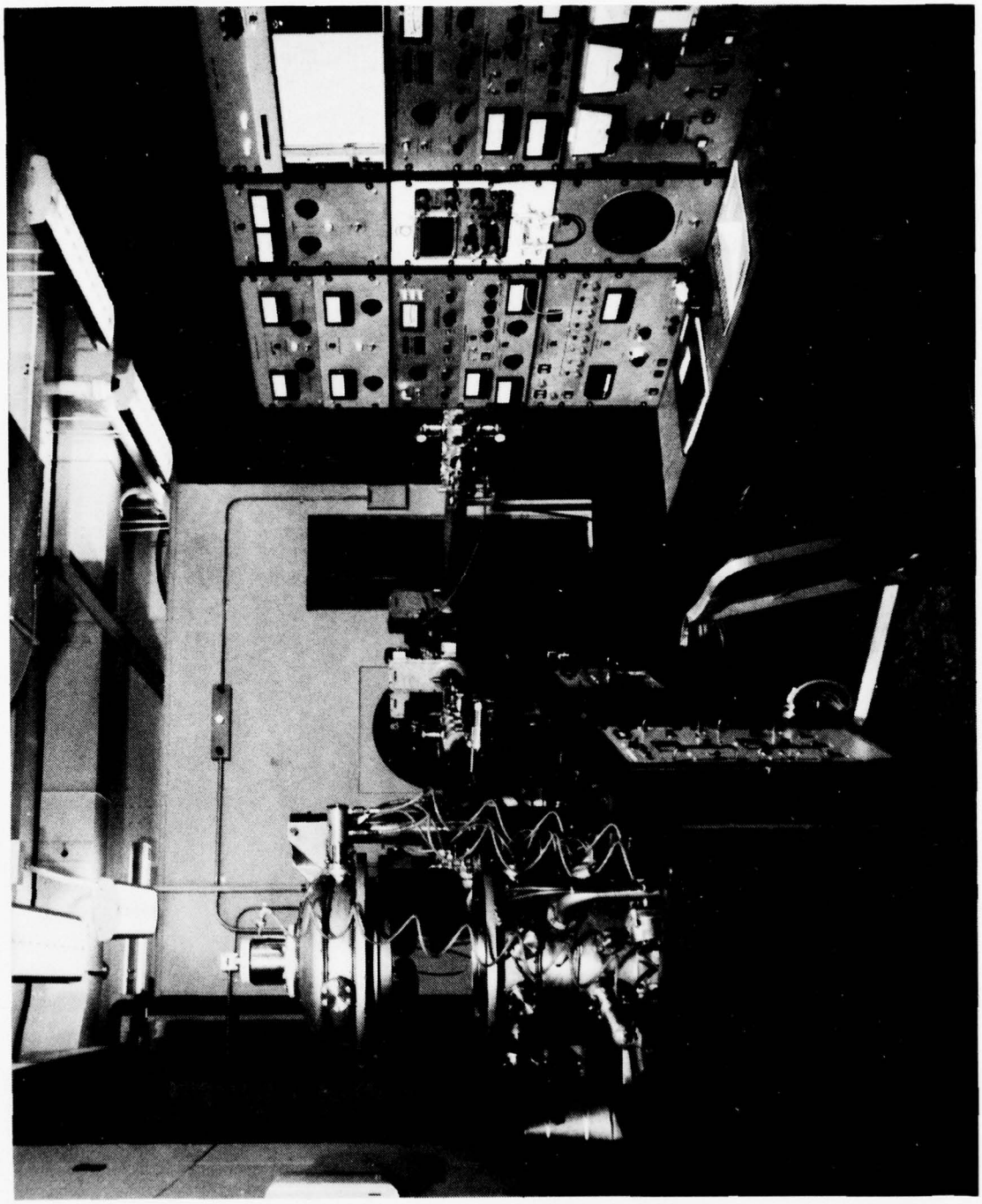

Figure 5. Photograph of ion-implantation facilities.

only by taking the wafers to wafer-process completion and then on to transistor fabrication and final high-frequency evaluation. This procedure is extremely slow, and only a few experimental tests could be completed within the duration of this program, jeopardizing the development of the ion-implantation procedure for use on this program.

The effort to develop a junction-delineation technique for ion-implanted junctions resulted in the use of a copper-sulfate solution developed at the RCA Laboratories in Princeton, NJ. This solution is composed of

(a) 35 milliliters of a saturated aqueous copper-sulfate solution,

(b) 10 milliliters of concentrated hydrofluoric acid, and

(c) 960 milliliters of water.

The solution is applied to a freshly lapped, highly polished sample under a high-intensity lamp. Care must be taken to avoid excessive plating of copper in order to obtain maximum junction resolution. Figure 6 illustrates the results achieved with this new junction-delineation procedure.

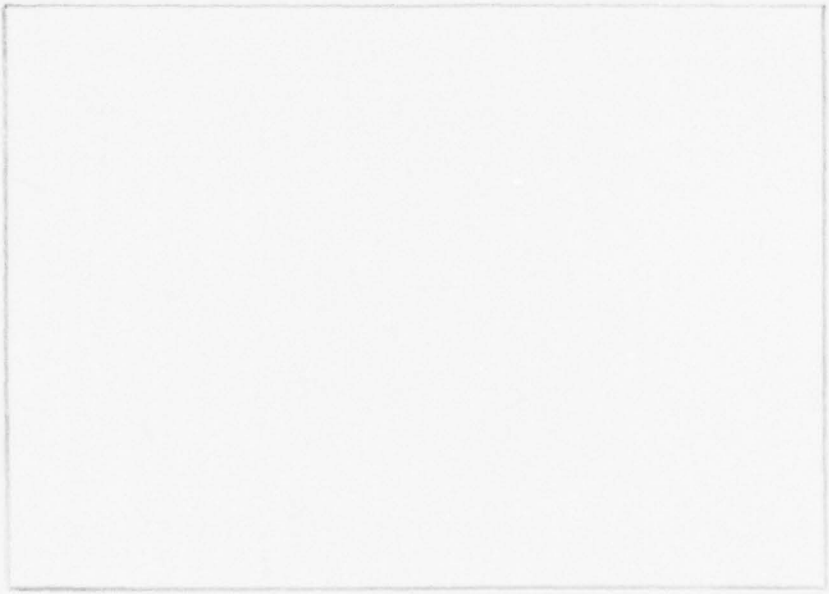

Figure 6. Ion-implanted n-p-n junctions delineated with copper staining.

When the experimental matrix was expanded to achieve a reduced base width, the reproducibility of the base-junction depth and, consequently, the base width was found to be poor. Also, junction-depth measurements showed that the base-junction penetration was deeper than predicted by the LSS [4] theory for ion implantation. The deeper base junctions could be accounted for by the boron diffusion which occurs during the anneal time for the base and emitter implants. Figure 7 shows the calculated base-impurity profile as it was after boron implantation and again after an anneal at 1000°C for 45 minutes. It is shown in these calculated impurity profiles that a 30% decrease in the base-junction depth can be achieved with a reduction in the base and emitter anneal schedules. Such a reduction in junction depth is very desirable because of the resultant abrupt impurity gradient of the base profile and of the narrower base width obtainable without punch-through.

A matrix of experiments for the exploration of a reduced emitter anneal schedule was described in the Second Interim Report [2]. That report also described a second matrix of experiments aimed at determining the minimum time needed to anneal the base. In this case, an oxide was deposited by the pyrolytic decomposition of silane after the base implant; it is necessary to densify this oxide prior to the emitter-pattern photolithography. This was done at a temperature of 800°C for 5 minutes. This condition was chosen because it would have the least effect on the base-junction depth. In this case, the samples were each annealed at either 900°C or 800°C for 15 minutes after emitter implantation. For each wafer, the emitter-junction depth of wafers annealed at 900°C is only slightly less than those annealed at 800°C for 15 minutes, even with the emitter-implant energy at different levels. The average base-junction depth is 0.36 μm and compares well with the computed base-impurity profiles shown in Fig. 7. The base junction shows only a 0.01-μm difference between the 800°C and 900°C anneal schedules.

Transistors fabricated from wafers 421-1R, 4B, and 2T, featuring a base impurity concentration of 5.0×10^{19} and an emitter implant energy of 160 keV, provided, in common emitter, a gain of 6.6 to 6.8 dB at 3 GHz, which satisfies the specifications for the commercial transistor type RCA 3003.

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4. J. Lindhard and M. Scharff, Physics Review 124, 128 (1961).

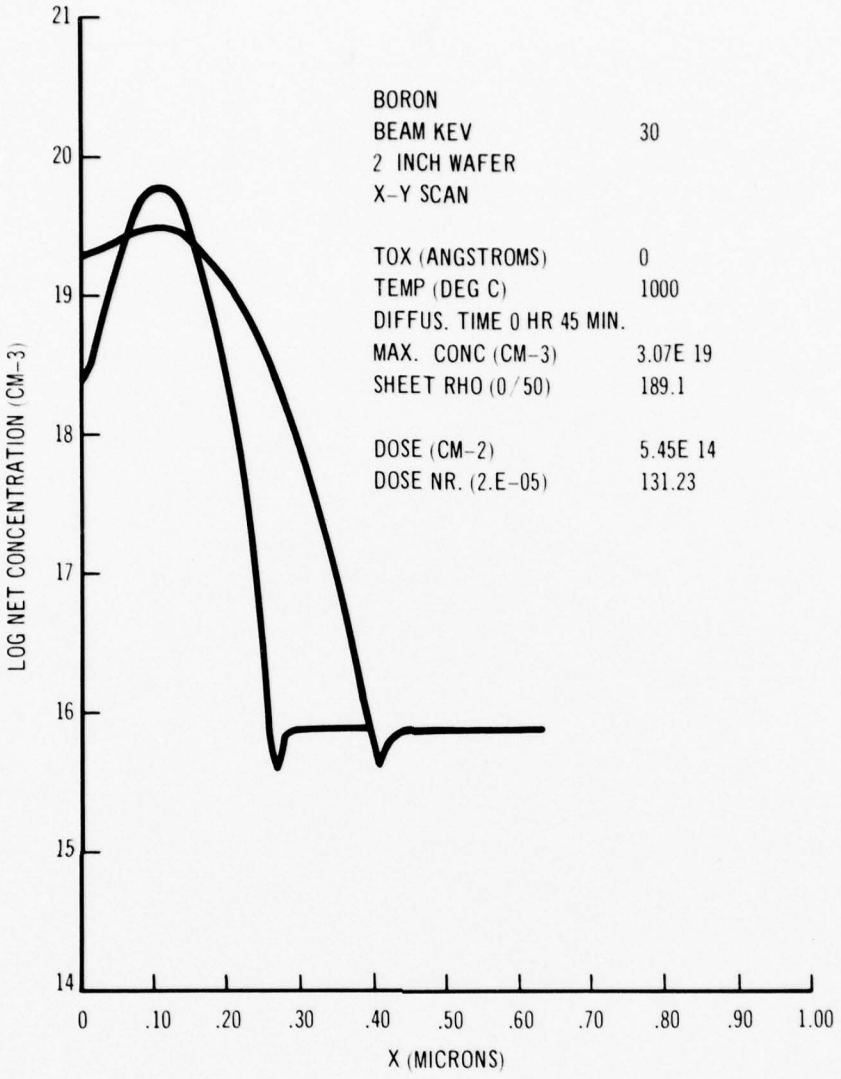


Figure 7. Calculated base impurity profiles after boron implantation and after annealing.

2. Ion Implantation on TA8791 Design

Everything that was learned from ion-implantation experiments on the TA8870 design was then applied to the new high-frequency design, the TA8791. In order to overcome some difficulties (emitter-to-base short-circuits) encountered previously in the TA8870 design and described in the Third Interim Report [3], the anneal temperature was raised to 1000°C while the time was

reduced to 15 minutes. This schedule was found to be a good compromise to obtain enough lateral diffusion of the emitter to overcome the emitter-base short-circuits and, at the same time, to retain a sharp base-impurity profile to produce a thin base region.

The new matrix of experiments with the L601 runs is shown in Table 2. Having fixed the base and emitter doping levels, and the annealing schedule, the intent of the experiment was to determine the best emitter dopant and the best ion energy. Some of the wafers were not completed because of damage during the processing, but one wafer, L601-3B, was processed successfully and provided some of the best rf results obtained with the TA8791 design. Most of the delivered large transistors (8 cell-pairs) were fabricated from this wafer.

Table 2. Ion-Implantation Matrix of Experiments

Wafer	Base		Emitter			Anneal	
	keV	N Max	Dopants	keV	N Max	Temp(°C)	Time(min)
L601-3T	30	2.5×10^{19}	As	150	5.0×10^{20}	1000	15
3B	30	2.5×10^{19}	As	150	5.0×10^{20}	1000	15
4T	30	2.5×10^{19}	As	150	5.0×10^{20}	1000	15
4B	40	2.5×10^{19}	P	40	5.0×10^{20}	1000	15
5T	40	2.5×10^{19}	P	40	5.0×10^{20}	1000	15
5B	40	2.5×10^{19}	P	40	5.0×10^{20}	1000	15
8T	30	2.5×10^{19}	As	110	5.0×10^{20}	1000	15
8B	30	2.5×10^{19}	As	110	5.0×10^{20}	1000	15

C. DOUBLE-LAYER EPITAXIAL MATERIAL

The epitaxial structure controls the device current-handling capability by fixing the point at which base widening occurs. The maximum current density is given by the equation

$$J_{max} = q \mu N \frac{V}{t}$$

$$= \frac{V}{\rho t} \qquad (1)$$

where

J_{max} is the maximum current density (A/cm^2)

V is the applied voltage (V)

ρ is the epitaxial resistivity (ohm-cm)

μ is the mobility ($cm^2/V\text{-}s$)

N is the epitaxial concentration ($atoms/cm^3$)

q is the electron charge (coulombs)

t is the epitaxial thickness (cm)

From this equation, it can be seen that the lower the product of epitaxial resistivity and thickness (ρt), the greater the current that can be handled before the onset of base widening. Double-epitaxial material allows the lowering of the ρt product without compromising the collector-base junction breakdown voltage.

The approach was successful since devices made from wafer L607-7 gave some of the best rf performances. The wafer features a sublayer with a resistivity of 0.15 ohm x cm and a top layer with a resistivity of 0.60 ohm x cm. The breakdown voltage was about 52 V which is well above the 36-V minimum required for operation in class A with a collector bias of 18 V.

D. THERMAL PROPERTIES

1. Ultra-Thin Pellets with Integral Heat Spreader

The importance of low thermal resistance for linear-microwave-transistor performance was discussed in the First Interim Report [1]. In these devices, thermal-resistance calculations indicate that more than 50% of the thermal resistance lies in the silicon chip. Therefore, a thinner silicon chip must be used if a significant reduction in thermal resistance is to be made.

RCA conducted a study for the Air Force Systems Command under Contract No. F33615-71-C-1845 in which it was shown that a reduction in the thickness of a silicon UHF transistor from 4.3 to 3.0 mils resulted in a 19% reduction in thermal resistance. Thinning wafers below 3.0 mils does not appreciably decrease the thermal resistance because the area of thermal interface becomes smaller; therefore, the thermal-flux density is increased as the pellet thickness is decreased. When the pellet is eutectic-mounted, the thermal resistance of the interface is high and the higher thermal-flux density limits the heat

flow from the pellet. If, however, the pellet is thinned and the silicon is replaced with a high-thermal-conductivity material such as copper, the flux density at the pellet thermal interface is maintained even with an ultra-thin pellet. Replacing the silicon with a copper heat spreader also provides a mechanical handle so that the wafer and pellets can be subsequently processed.

A technique to apply a plated, integral heatsink to an ultra-thin pellet was developed at the Microwave Technology Center (MTC) of the RCA Laboratories. Experimental wafers for this program were supplied by the RF and Microwave Devices Group of the Solid State Division.

After a few experimental runs on dummy wafers, the mechanics of the process were solved. The major problem areas were: the obtaining of a uniformly thin wafer, a metallization schedule that allowed stressless attachment of the heatsink, and a high-yield dicing technique. Furthermore, a new low-temperature deposition process was developed for metallization of the copper back which reduces the difficulties in pellet mounting that had been experienced with earlier samples. In the new process, the wafer is wax-mounted onto a sapphire disc and back etched to 0.5 mil; then successive layers of chromium, palladium, and copper are deposited directly onto the freshly etched wafer. In this process, the palladium layer acts as a barrier, separating the copper from the silicon. This barrier eliminates the undesirable intermetallics obtained when copper and silicon are in direct contact and results in a much improved metallurgical system. The process was then applied to wafers of TA8870 and TA8791 transistors.

Portions of these wafers were saved in their original state and were later used to compare thermal and electrical characteristics. The sketch in Fig. 8 shows both the standard-commercial-pellet attachment and the plated-heatsink-pellet attachment. Type TA8870 single-cell transistors, under dc dissipation conditions, showed a 2-to-1 improvement in hot-spot thermal resistance - from 26°C/W for the standard pellet to 13°C/W for the integral-heatsink pellet. The improvement was only about 15% for type TA8791 because this latest design, without plated heatsink, already has a hot-spot thermal resistance of about 14°C/W. The dc characteristics of both transistor types were apparently unaffected.

Plated heatsink devices fabricated from wafers L605-6 and L607-7 have been delivered.

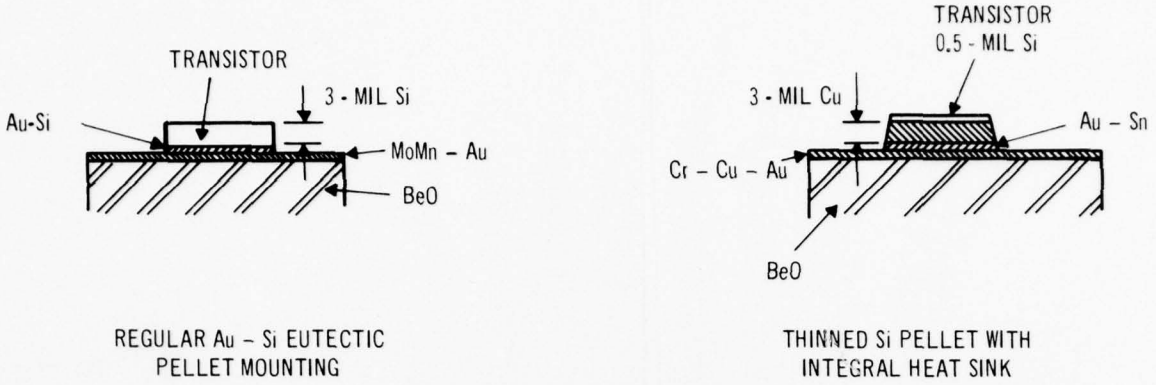


Figure 8. Transistor heatsinking.

2. Thermal Measurements with Infrared Microscope

In order to operate successfully, large transistors in class A must not only have a low thermal resistance between the junction area and the heatsink, but must also have an even distribution of the bias current throughout the various cells of the transistor. Provided the pellet is properly mounted, this results in a uniform distribution of the temperature on the surface of the transistor. Emitter-ballasting is the key parameter controlling the current distribution, and its value must be kept to a minimum, thus providing an acceptable temperature distribution without introducing excessive rf losses. The use of a computer-controlled infrared microscope allowed the optimization of the emitter-ballasting and the measurement of thermal resistance of plated heatsink and regular devices.

The instrument consists of an infrared microscope with an InSn detector, a stage driven by stepping motors, and a temperature controller. The whole system operates under the control of a minicomputer as shown in Fig. 9; a photograph of the system is shown in Fig. 10. The stepping motors can rapidly position the stage to an accuracy of 1/16 of a mil in the X-Y plane. A temperature scan of a semiconductor device is obtained as described below. The

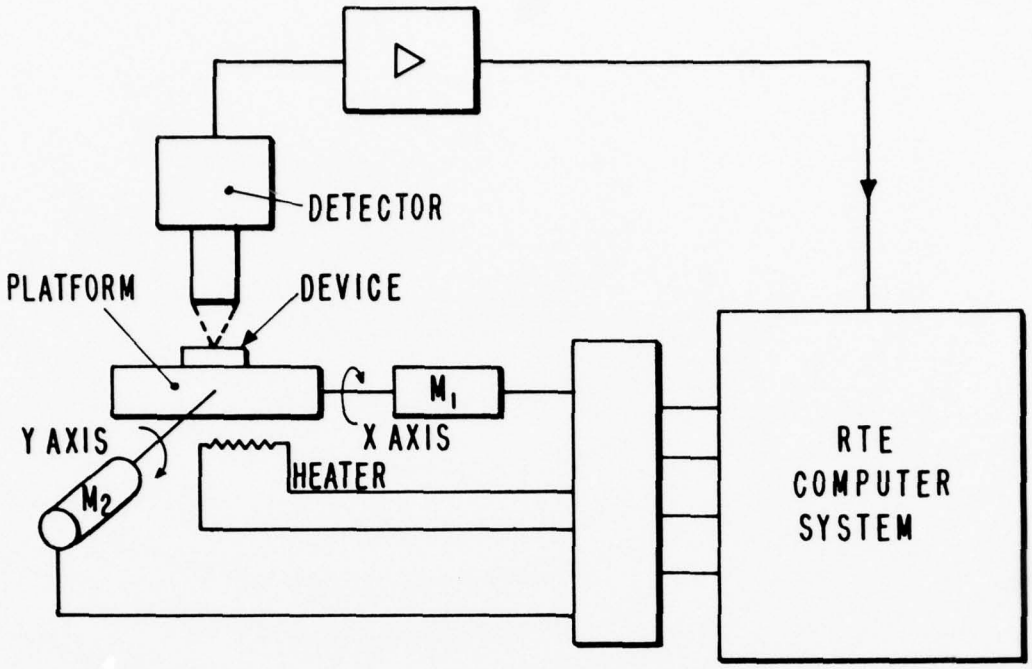


Figure 9. Block diagram of computer-controlled infrared microscope.

device is mounted on the stage and brought to a uniform elevated temperature by a heater in the stage. The device is then automatically scanned, and the readings for every spot along the scan are stored in the computer (the spot resolution is approximately 1.5 mils). This procedure is repeated for several other temperatures, and, from the infrared emission data obtained this way, the emissivity of every scanned spot on the device is calculated by the computer and stored in its memory. DC power and, in the case of rf amplifying devices, rf power are now applied to the device, and a final scan is made with the microscope. The computer takes the readings from this scan, converts them to temperature using the stored information on the surface emissivity of the device, and produces a plot of device temperature vs distance. The whole procedure takes approximately 1/2 hour.

The temperature profiles of the four cells of a 6-cell-pair device type TA8791 are shown in Fig. 11. The large temperature difference between the various cells indicates insufficient ballasting for class A operation. Figure 12 shows the temperature profiles of a similar device that can operate satisfactorily in class A.

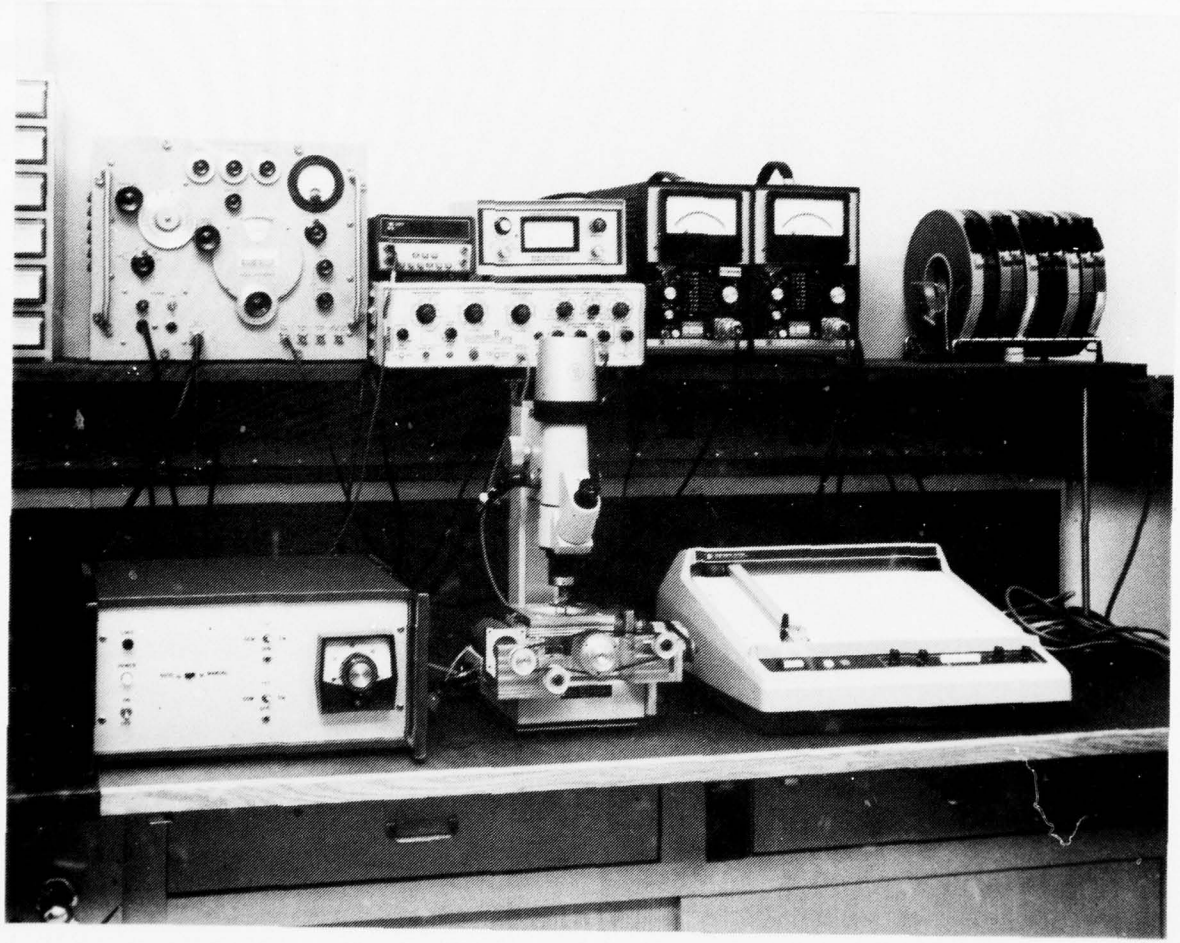


Figure 10. Photograph of computer-controlled infrared microscope.

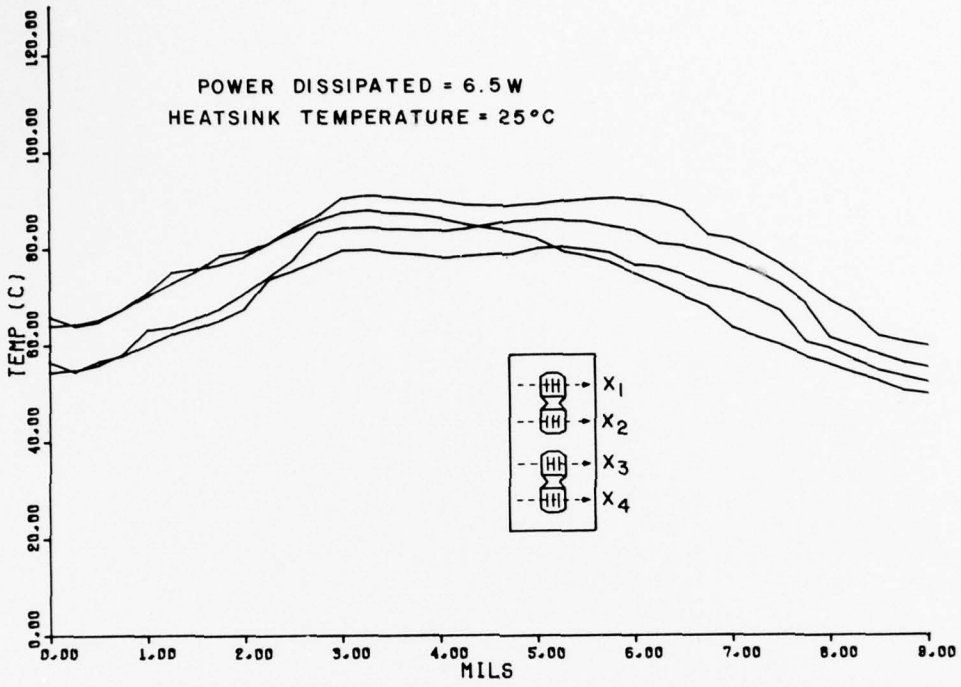


Figure 11. Uneven temperature distribution - TA8791 transistor.

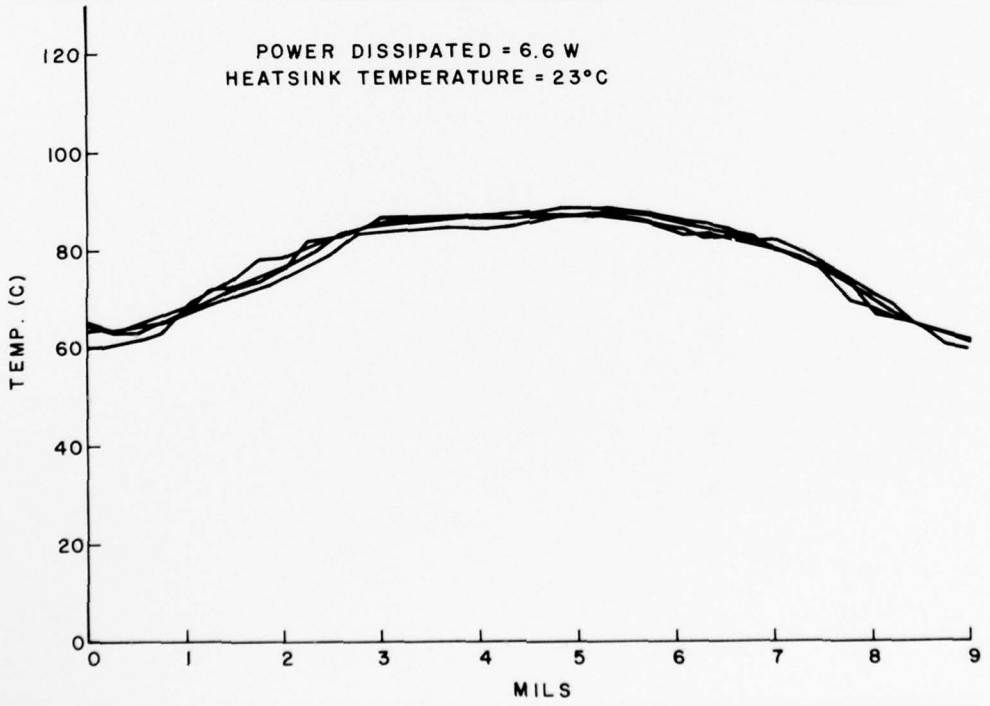


Figure 12. Even temperature distribution - TA8791 transistor.

E. MICROSTRIP BeO CARRIERS AND MOM CAPACITORS

In order to obtain optimum rf performance with large multiple-cell transistors, a new BeO microstrip carrier was used. This carrier, developed under Contract No. DAAB07-72-C-0225 for the U. S. Army Electronics Command, consists of two BeO parts joined with a low-loss diffusion braze as shown in Fig. 13. The joint serves as the ground connection without inhibiting the spreading of the heat from the area where the pellet is mounted. The carriers are fabricated by starting with two 1-inch by 1-inch polished and Cr-Cu metallized BeO wafers. These are pressed together with metal clamps and diffusion bonded under heat in an inert atmosphere. The composite wafer is subsequently sliced, and the resulting strips are metallized and etched for the desired pattern. The strips are then cut into separate carriers. The thin-film Cr-Cu-Ag-Au metallization on these carriers allows an excellent pattern definition, low electrical and thermal resistances, and good interfacing with the Au-Sn eutectic used to mount the transistor pellets on the carriers.

A low-impedance transmission line at the input provides the necessary impedance transformation from the transistor pellet to the 50-ohm generator. The output tuning is provided by a shunt inductor, L (see Fig. 13), connected between the base of the transistor and a dc-blocking capacitor, C, mounted on the collector contact. Shunt tuning of the output capacitance directly on the carrier is essential for optimum broadband performance of the amplifier. Because of the high rf current flowing through capacitor C, it is very important that its losses are low.

RCA MOM (metal-oxide-metal) capacitors with a thermally grown SiO_2 layer are approximately five to ten times better than similar MOS capacitors. They are fabricated by growing a 1-μm layer of SiO_2 on the silicon substrate followed by an evaporation of a thin film of Cr-Cu. The wafer is then copper-plated up to a thickness of 5 mils, and the silicon substrate is etched to expose the SiO_2 layer. A Cr-Cu film is deposited on the SiO_2, and the electrodes are defined with a standard photolithographic technique. The high quality of the thermally grown SiO_2 and the replacement of the lossy silicon substrate with a copper electrode are the key factors for the excellent electrical performance of these capacitors. As an example, at 3.0 GHz, the Q of a 60-pF MOM capacitor is about 40 while the Q of a similar MOS capacitor is about 5.

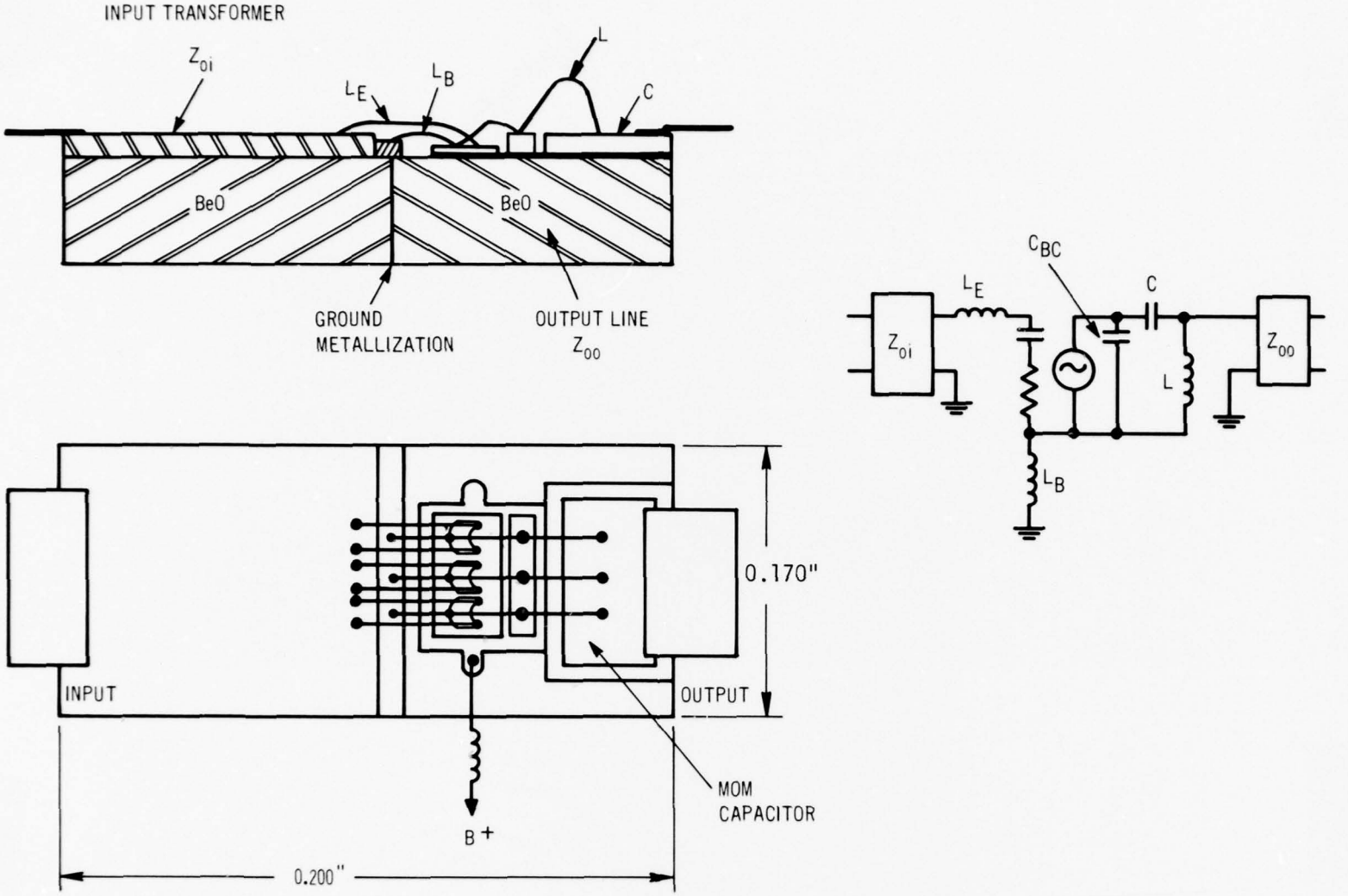


Figure 13. BeO microstrip carrier.

Figure 14 shows the photograph of an 8-cell-pairs transistor pellet mounted on a BeO carrier. The MOM capacitor, the tuning inductances L, and the input transformer are clearly visible on the picture.

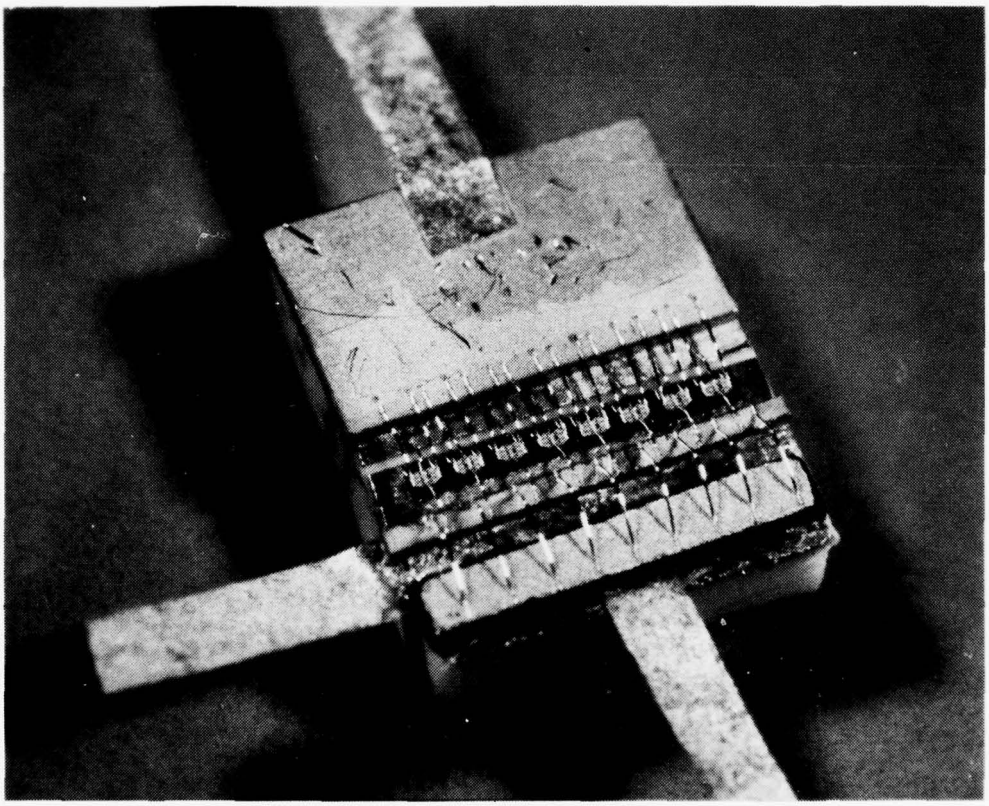
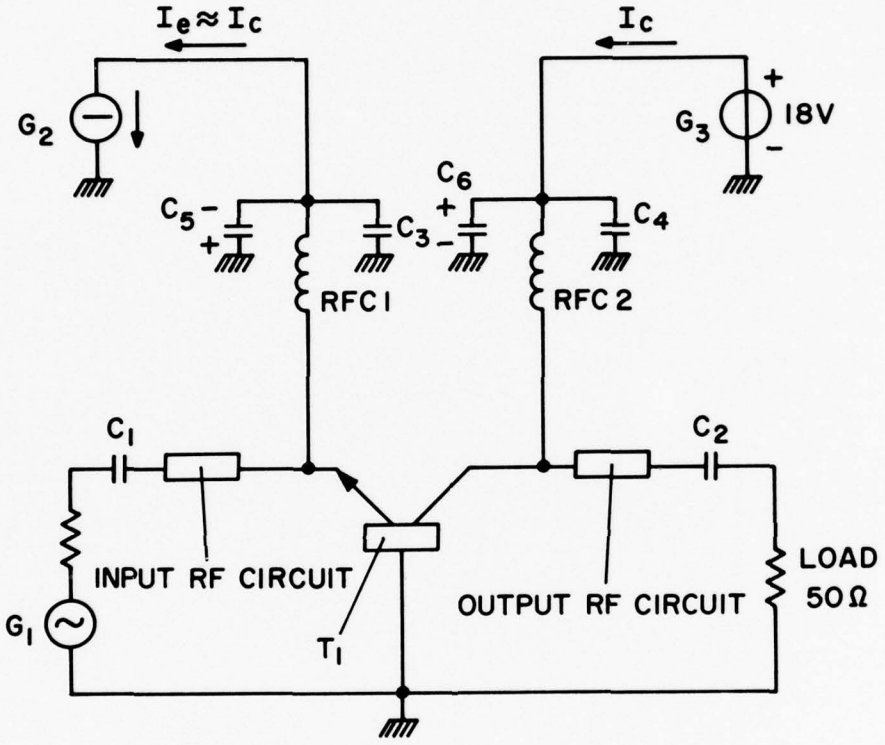


Figure 14. Photograph of TA8791 - 8 cell-pairs on BeO carrier.

F. TRANSISTOR RF EVALUATION

The transistors, made with pellets mounted on the carriers described in Section II.E. above, were connected on a microstrip test circuit and tuned for best performances at specified frequencies. Since the tuning was performed with stubs located on the microstrip circuit and physically close to the active device, the losses caused by high standing wave ratios were kept to very low values. The electrical schematic of the bias circuit is shown in Fig. 15 and features a constant voltage generator to bias the collector and a

constant current generator to bias the emitter. The collector current is therefore constant and independent from the rf drive, which is a requirement for true class A operation. A bias point of 18 V and 120 mA per cell-pair was found experimentally to provide the best efficiency. A bias of 18 V and 960 mA was therefore used for 8-cell-pairs devices.



G_1 = RF GENERATOR
G_2 = CONSTANT CURRENT DC POWER SUPPLY
G_3 = CONSTANT VOLTAGE DC POWER SUPPLY

C_1, C_2, C_3, C_4 = MOM CAPACITORS - 30 pF
C_5, C_6 = ELECTROLITIC CAPACITORS - 15 μF
T_1 = TRANSISTOR UNDER TEST

RFC1, RFC2 = RF CHOKES

Figure 15. Electrical schematic of test circuit.

The performances of the delivered transistor samples are summarized in Table 3, and Fig. 16 shows typical P_{out} vs P_{in} characteristics for an 8-cell-pairs device operating at 3.0, 3.6, and 4.0 GHz.

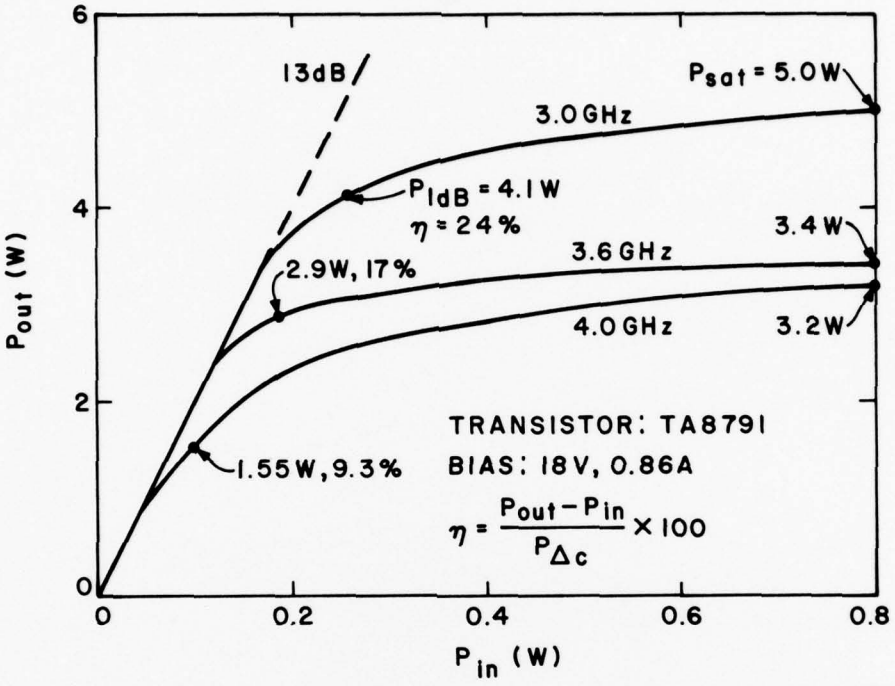


Figure 16. Saturation characteristics - TA8791 8 cell-pairs.

Most of the delivered transistors (8 out of 12) were fabricated from wafer L601-3. This wafer was made with the most advanced ion-implanted techniques, and it was gratifying to see that its performance was among the best obtained with the TA8791 design. Some of the features of the L601 wafer and of other wafers are summarized in Table 4. Good performances were also obtained from wafer PH607-7. This wafer features a double-epitaxial layer, as described in Section II.C. above, and a plated heatsink with a copper thickness of 3 mils. The thickness of the silicon pellets is about 0.5 mil. A common characteristic of the other two wafers, L615-4R and PH605-6, is the use of gold for the metallization pattern. As was mentioned in Section II.A., transistors with gold metallization are expected to provide higher rf output power than transistors having aluminum metallization because of lower rf losses and improved current-handling capability.

Table 3. RF Performances of Delivered Sample Transistors

Device No.	Wafer No.	Bias Voltage (V)	Bias Current (A)	Operating Frequency (GHz)	P_{sat}* (W)	$P_{1\ dB}$* (W)	η_{sat}* (%)	$\eta_{1\ dB}$* (%)	Small-Signal Gain (dB)	No. of Pairs
9	L615-4R	18.0	0.85	3.5	3.9	-	20.2	-	-	7
9	L615-4R	18.0	0.85	4.0	3.5	1.0	17.6	6.4	13.2	
11	L615-4R	18.0	0.96	3.6	4.0	3.0	18.5	16.7	14.7	8
11	L615-4R	18.0	0.96	4.0	3.5	2.4	15.6	13.2	12.4	
13	PHL607-7	18.0	0.96	3.5	3.4	2.7	15.0	14.8	13.0	8
13	PHL607-7	18.0	0.96	4.0	2.5	1.2	10.1	6.8	13.5	
14	L601-3	18.0	0.86	3.5	4.0	3.2	25.8	20.6	11.5	7
14	L601-3	18.0	0.86	4.0	3.0	1.7	19.8	11.3	12.4	
15	L601-3	18.0	0.86	3.7	3.3	2.8	17.0	15.8	10.2	7
15	L601-3	18.0	0.86	4.0	3.2	2.0	16.0	12.0	18.8	
19	L601-3	18.0	0.96	3.5	3.2	2.5	13.8	12.1	9.2	8
19	L601-3	18.0	0.96	4.0	3.0	1.2	12.7	6.7	13.2	
20	L601-3	18.0	0.96	3.4	3.7	3.0	16.7	15.3	10.0	8
20	L601-3	18.0	0.96	4.0	3.4	0.7	15.0	4.3	18.3	
24	PH605-6	18.0	0.96	3.4	3.3	3.1	14.4	15.3	9.0	8
24	PH605-6	18.0	0.96	4.0	3.0	0.9	12.7	4.8	12.3	
27	L601-3	18.0	0.84	3.5	3.5	2.2	18.5	14.4	15.8	8
27	L601-3	18.0	0.84	4.0	3.3	1.6	17.2	10.9	18.8	
30	L601-3	18.0	0.84	3.6	3.1	2.0	15.8	12.2	13.5	8
30	L601-3	18.0	0.84	4.0	3.0	1.4	15.5	9.2	12.2	
34	L601-3	18.0	0.96	3.4	3.2	2.8	13.9	13.6	8.7	8
34	L601-3	18.0	0.96	4.0	3.2	1.5	13.8	8.5	12.7	
35	L601-3	18.0	0.96	3.4	3.1	2.5	13.3	12.9	9.7	9
35	L601-3	18.0	0.96	4.0	2.9	1.0	12.1	5.8	19.0	

*P_{sat} is the output power of saturation; $P_{1\ dB}$ is the output power at 1-dB compression point; η_{sat} is the power-added efficiency at saturation; and $\eta_{1\ dB}$ is the power-added efficiency at 1-dB compression point.

Table 4. Summary of Wafer Characteristics

Wafer No.	Epi-thickness (mils)	Epi-resistivity (Ω x cm)	LTD Resistance (Ω x square)	Diffusion Process	Metal-lization
L601-3	0.29	0.54	270	ion implanted	aluminum
PH605-6 plated heatsink	0.29	0.66	301	S5	gold
PH607-7 plated heatsink	sub layer:0.20 top layer:0.30	0.15 0.60	226	S5	aluminum
L615-4R	0.28	0.5	272	S5	gold

SECTION III

AMPLIFIER DEVELOPMENT

A. DESIGN PROCEDURE

In a high-power transistor amplifier, the amplitude of the signal is large enough to cause changes in the parameters of the transistor. Consequently, the characterization of the active device by small-signal parameters is not sufficient for the design of the amplifier. In particular, the saturation characteristic, or change of the gain as a function of the input rf drive, depends on both the device parameters and the microwave circuit in which the transistor is imbedded. Having optimized the device parameters for high output power in class A operation and for good distribution of the bias current between the various cells, the microwave circuit has to be optimized for best linear operation. Considering, for instance, the simplified set of collector characteristics shown in Fig. 17, it can be proven [5] that the best load resistance for highest linear output power is given by

$$R_L = \frac{V_{cc} - V_{sat}}{I_{cc}} \tag{2}$$

where V_{cc} and I_{cc} are the bias voltage and current, respectively, and V_{sat} is the saturation voltage. A higher or lower value of R_L will cause either a premature current saturation or rf voltage clipping. Similarly, if one considers, for instance, the S parameter S_{21} (gain) of the transistor as a function of the collector voltage and current, Fig. 17(b), it becomes clear that different load lines will be characterized by different changes of the S parameters along each line [6]. Since the load line is the locus of the instantaneous operating points, variation of the S parameters will cause variation of gain with consequent distortion.

Although this analysis is very simplified because in the actual transistor the large collector-base capacitance will affect the collector

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5. R. Thorton et al., Handbook of Basic Transistor Circuits and Measurements, SEEC Vol. 7, (John Wiley and Sons, Inc., New York, 1966).
6. R. Bell and R. Clarks, "Elimination of Cross-Modulation in CATV Amplifiers," 21st Annual Convention, National Cable Television Association, Chicago, Illinois, May 14-17, 1972.

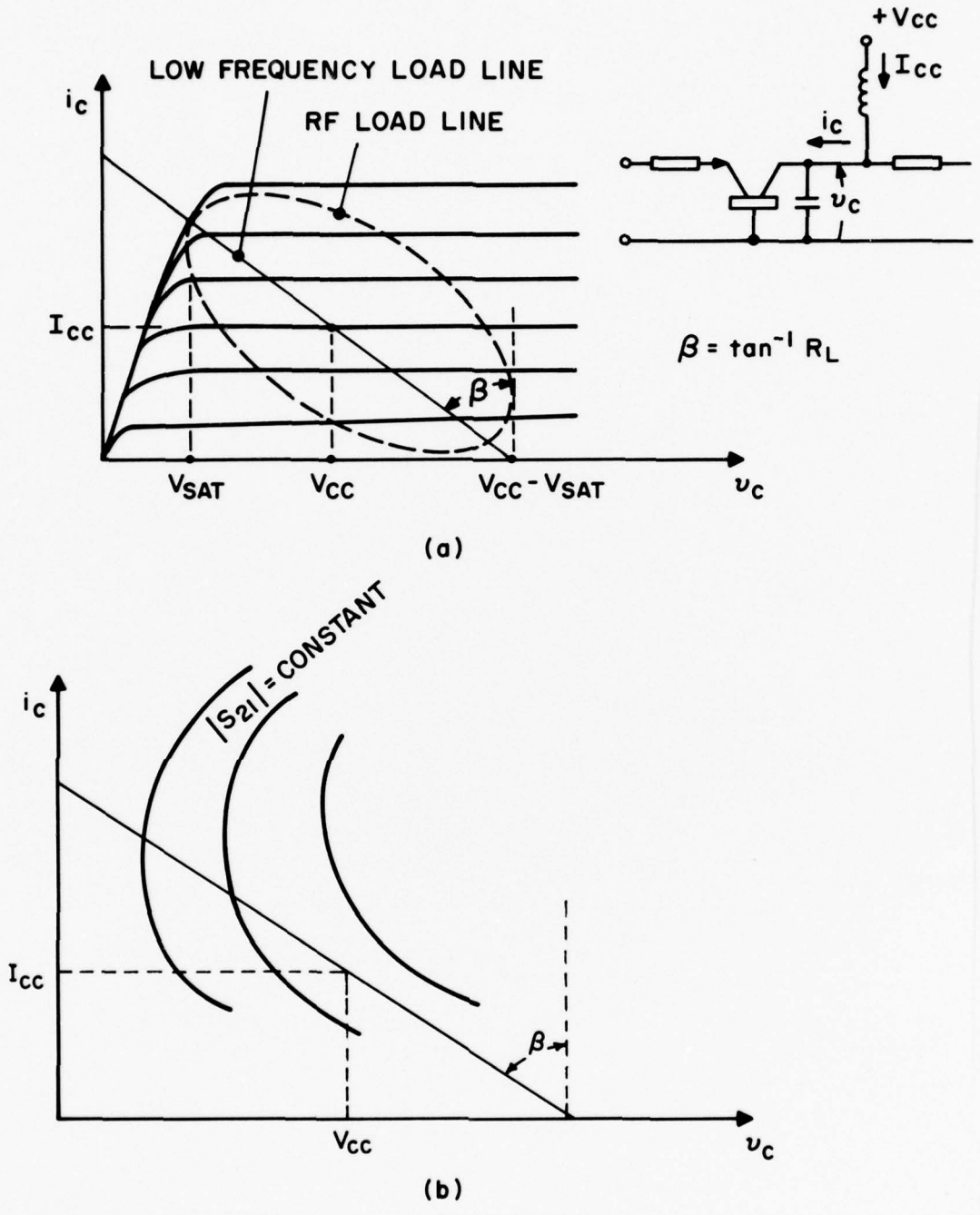

Figure 17. Load line for linear operation.

voltage-current relationship and the actual rf load line will be an ellipse (dotted line), this reasoning does show the existence of an optimum collector loading for best linear power. The rf load line and the gain are both functions of frequency, which explains the observed strong dependence of the linearity from the operating frequency as was described in the Third Interim Report [3].

Consequently, the adopted design procedure for the microwave circuit was as follows:

(a) Measure at discrete frequencies the load impedances for best output power and linearity.
(b) Sinterize and optimize the output circuit to present to the transistor a load that best follows the optimum load impedance vs frequency.
(c) Measure the small-signal S parameters of the transistor.
(d) Sinterize and optimize the input circuit of the amplifier for constant gain over the desired frequency band. The amplifier now comprises an input circuit (to be optimized), the transistor S parameters (fixed), and the output circuits (fixed).

This procedure is similar to the one described in Ref.[7] and relies on the fact that only the input circuit can be varied to obtain the desired gain vs frequency response, while the output circuit must be designed for maximum linear output power.

B. CIRCUIT DESIGN

1. Output Circuit, Single Transistor

The optimum load impedance (Z_{Lopt}) for a single 8-cell-pairs transistor operating at 18 V and 960 mW is shown in Fig. 18. The transistor is mounted on the microstrip carrier described in Section II.E. above. The shunt inductor, located on the carrier, is such as to resonate with the collector-base capacitance at a frequency of about 3.7 GHz. At this frequency, the real part of the optimum load impedance Z_{Lopt} assumes its maximum value.

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7. A. Presser and E. Belohoubek, "1-2 GHz High-Power Linear Transistor Amplifier," RCA Review 33, 737 (1972).

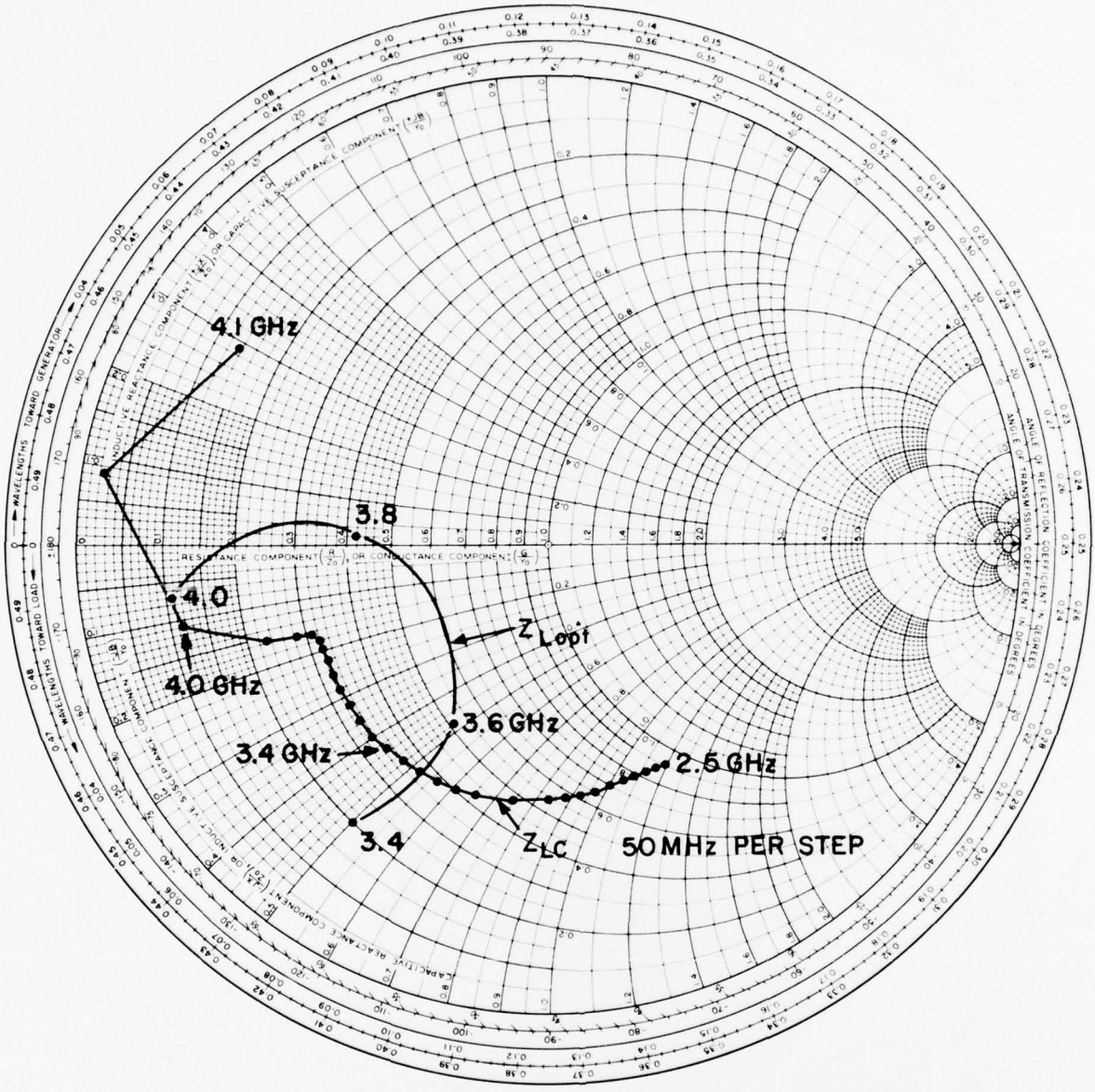

Figure 18. Output circuit - single transistor.

Because of the large output capacitance of these devices (15 pF for an 8-cell-pairs circuit), the impedance Z_{Lopt} varies rapidly with frequency, as shown in Fig. 18.

The task of designing an output circuit whose impedance best approximates Z_{Lopt} is a difficult one. Standard low-pass-type matching circuits cannot

match this transistor over a wide band because of their unfavorable relationship between frequency and impedance. A better circuit was designed which features two resonators offset in resonance frequency. The impedance vs frequency presented by this circuit to the transistor is such that, when the impedance is represented on the Smith chart, it has a cusp-like shape. The impedance (Z_{Lc}) of this type of circuit follows well the optimum load impedance Z_{Lopt} as shown in Fig. 18.

2. Input Circuit, Single Transistor

The small-signal S parameters of the transistor have been measured over the 3.0- to 4.0-GHz frequency range and are listed in Table 5. These data, together with the already fixed output circuit, have been used to design the input circuit with a goal of 10-dB gain over the 3.4- to 4.0-GHz frequency range.

Table 5. S Parameters of Transistor TA8791, 8 cell-pairs

FREQ (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
3000.0	.926	-179	.271	13	.044	65	.852	139
3100.0	.926	178	.327	5	.049	61	.826	127
3200.0	.924	177	.395	-2	.053	58	.834	116
3300.0	.921	175	.487	-11	.057	54	.835	107
3400.0	.912	173	.615	-21	.060	50	.781	98
3500.0	.901	171	.814	-32	.064	47	.669	86
3600.0	.884	170	1.144	-45	.071	44	.569	60
3700.0	.846	169	1.923	-70	.087	35	.677	4
3800.0	.872	173	2.531	-130	.093	3	1.032	-95
3900.0	.915	171	1.506	-173	.047	-1	.889	179
4000.0	.900	170	.958	170	.041	20	.932	146

Bias: 18 V, 960 mA

The input circuit consists of a two-step $\lambda/4$ transformer which reduces the 50-ohm impedance of the generator to the low level (approximately 3 ohms) necessary to drive the transistor. Figure 19 shows the generator impedance (Z_{ic}) as seen from the transistor terminals. On the same figure is shown the input impedance (Z_{in}) of the amplifier: the input VSWR is within a 2.5:1 ratio over the 3.4- to 4.0-GHz frequency range.

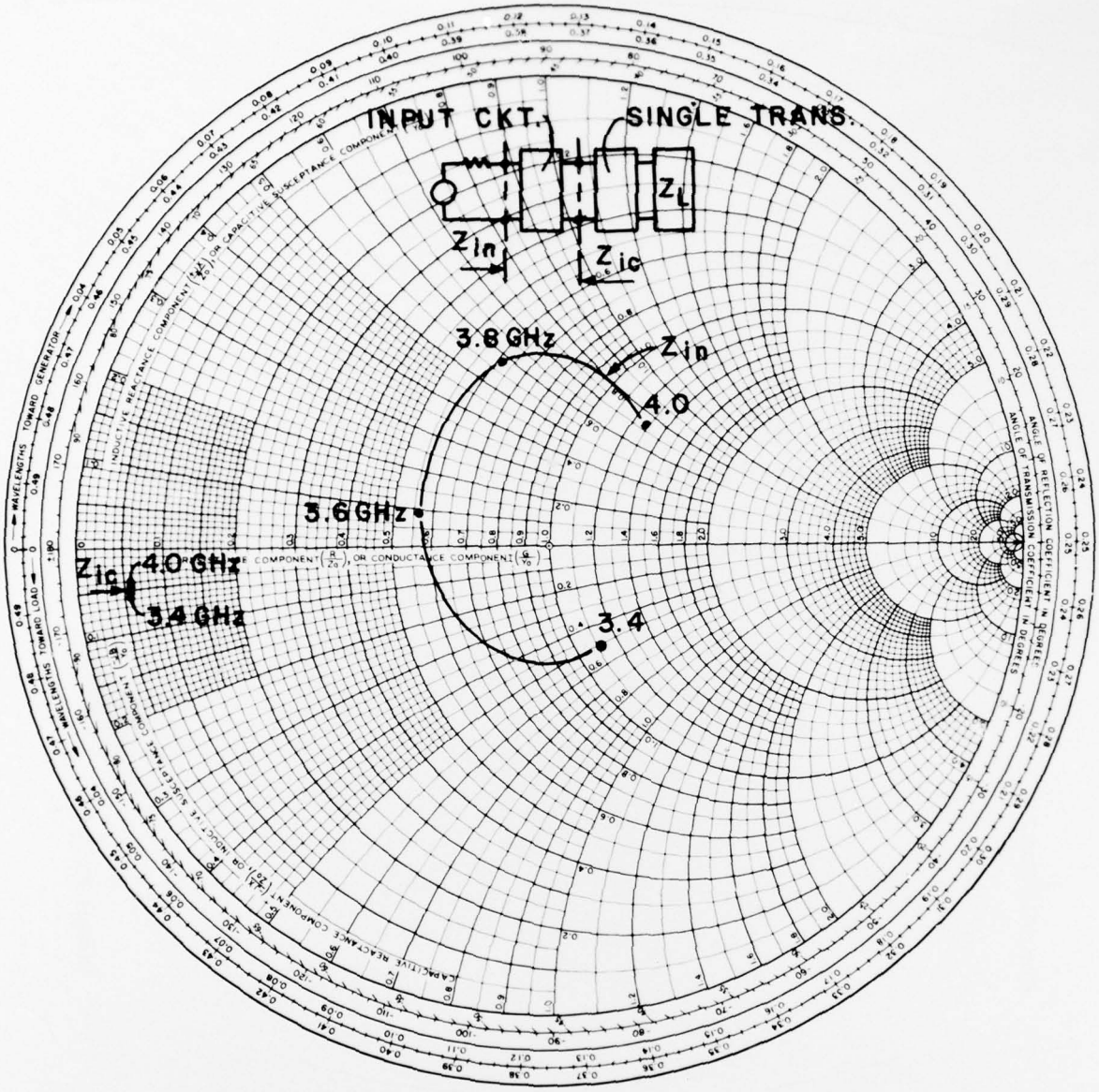

Figure 19. Input circuit - single transistor.

3. Input and Output Circuits, Two Transistors in Parallel

The full output power of 5.0 W at 4 GHz had to be obtained by operating two TA8791 transistors connected in parallel on the microwave circuit. The S parameters and the optimum load impedance for the combined transistors were

computed from data obtained on a single transistor. The input and output circuits were then designed following the procedure described previously.

The optimum load impedance (Z_{Lopt}) and circuit load impedance (Z_{Lc}) are plotted as functions of frequency in Fig. 20. Figure 21 depicts the impedance presented by the circuit at the input of the transistor (Z_{ic})

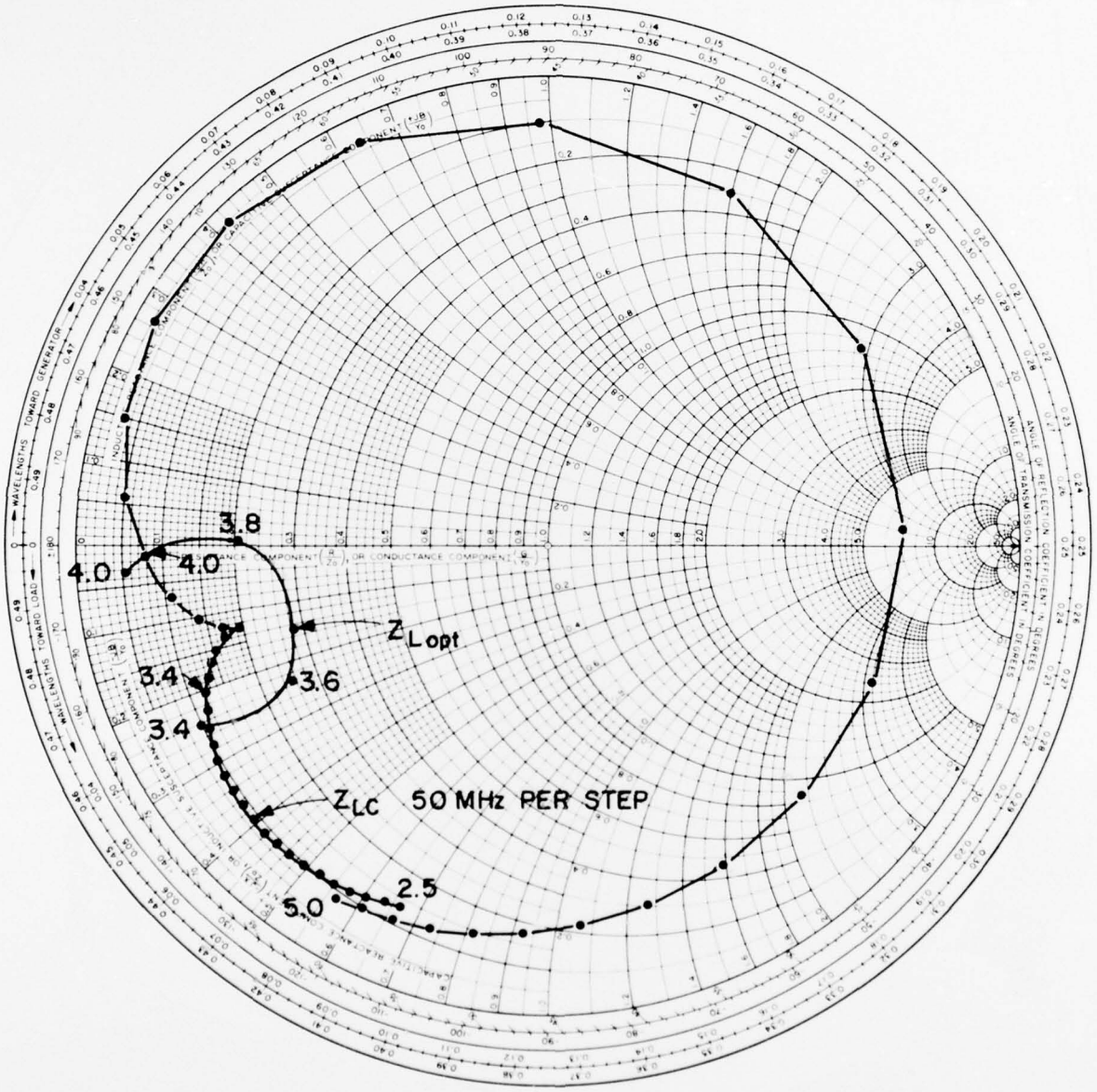

Figure 20. Output circuit - two transistors in parallel.

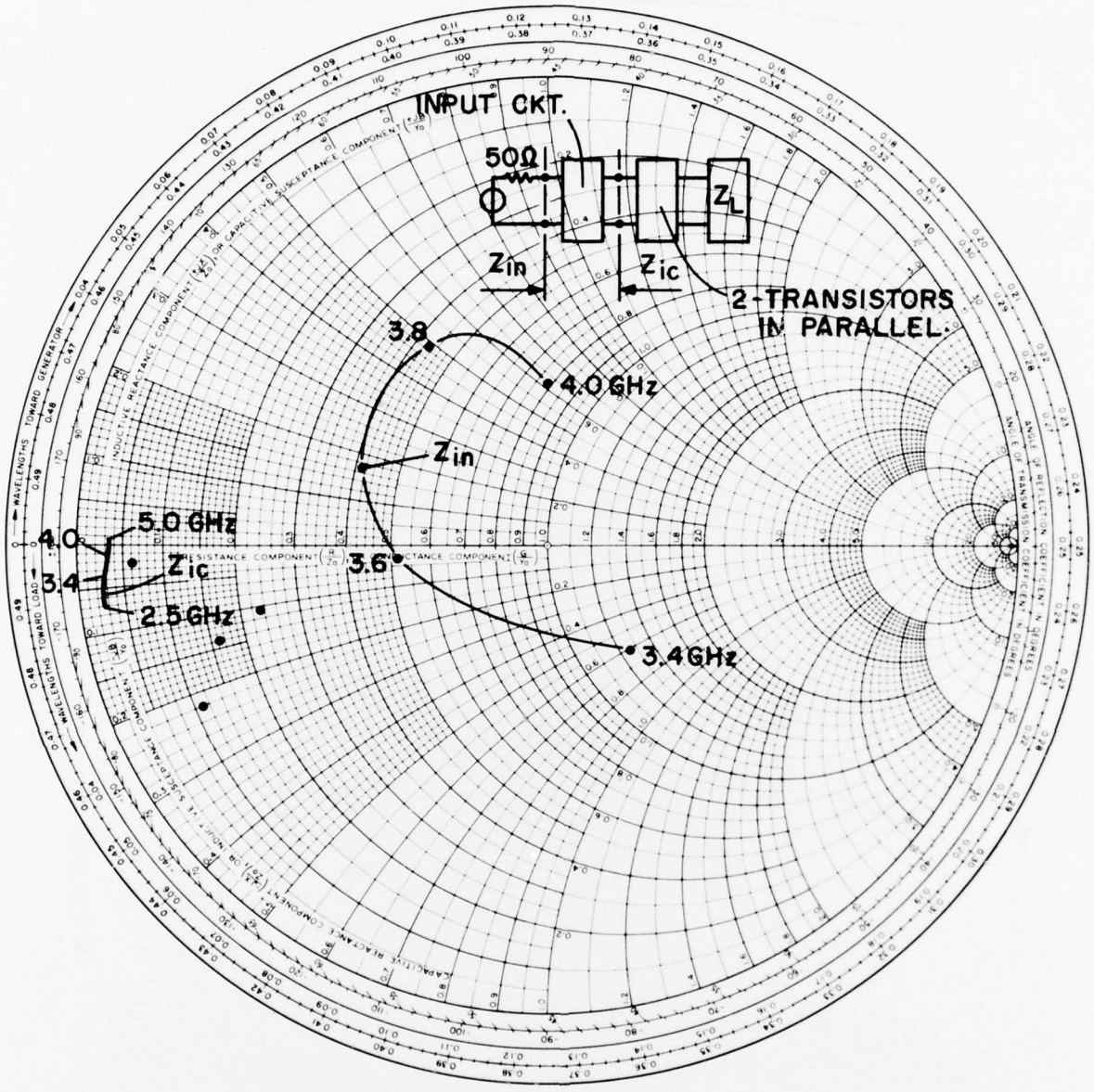

Figure 21. Input circuit - two transistors in parallel.

and the input impedance of the entire amplifier (Z_{in}). The Z_{ic} plot shows that the input impedance of the transistor is very low, only 1.5 ohms. It can be seen, on the Z_{in} plot, that the VSWR is better than 2.8:1 over the 3.4- to 4.0-GHz frequency range.

C. BROADBAND AMPLIFIERS PERFORMANCE

1. Single-Transistor Amplifier - Electrical Performances

The design of a broadband amplifier operating from 3.4 to 4.0 GHz was implemented using a single 8-cell-pairs transistor, listed as No. 34 in Table 3. The device was biased as shown in Fig. 15; a constant current dc supply in the emitter circuit provides a constant collector current for true class A operation.

The rf output power of the amplifier for a constant rf input power is shown in Fig. 22. The bandwidth at the 1-dB points extends from 3.34 to 3.95 GHz which is close to the design objective of 3.4 to 4.0 GHz. The slight downward shift in frequency is due to discontinuities at the end of the resonators that are part of the microwave circuit. The shunt inductor on the transistor carrier was resonating with the collector-base capacitance (C_{ob}) at a frequency of 3.7 GHz. This frequency was chosen as a compromise for good performances at 4 GHz and at the same time reasonably high gain at 3.4 GHz. The goal was 10-dB gain over the frequency band. The output power at the 1-dB compression point (linear power) peaks at the low end of the frequency band and is above the goal of 2.5 W over a range of 250 MHz. The rapid fall-off of the linear power at the high frequencies is typical of these devices, as was described in the Third Interim Report [3].

Curves of rf output power vs input power at discrete frequencies are shown in Figs. 23 and 24. The straight lines represent the extrapolation of the linear region and define the small-signal gain while the output power for 0.8 W of rf input power is defined as saturated power (P_{out}sat). The power at the 1-dB compression point (P_{out}1 dB) is also shown on these plots. The values for discrete frequencies of P_{out}sat and P_{out}1 dB together with the respective power-added efficiencies are listed in Table 6.

2. Dual-Transistor Amplifier - Electrical Performances

The electrical schematic of the amplifier using two transistors in parallel is depicted in Fig. 25. The two emitter circuits are in parallel for the rf signal but isolated for the dc. Two separate 1-ohm resistors are then used to divide the bias current equally between the two transistors. The measured performances of the amplifier whose design is described in

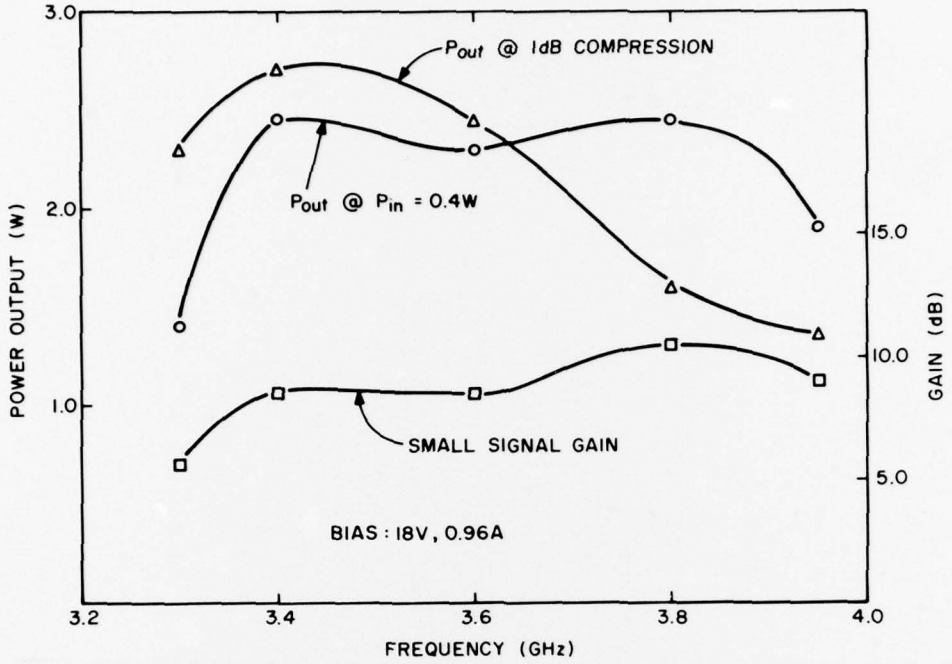

Figure 22. P_{out} and gain vs frequency - single transistor.

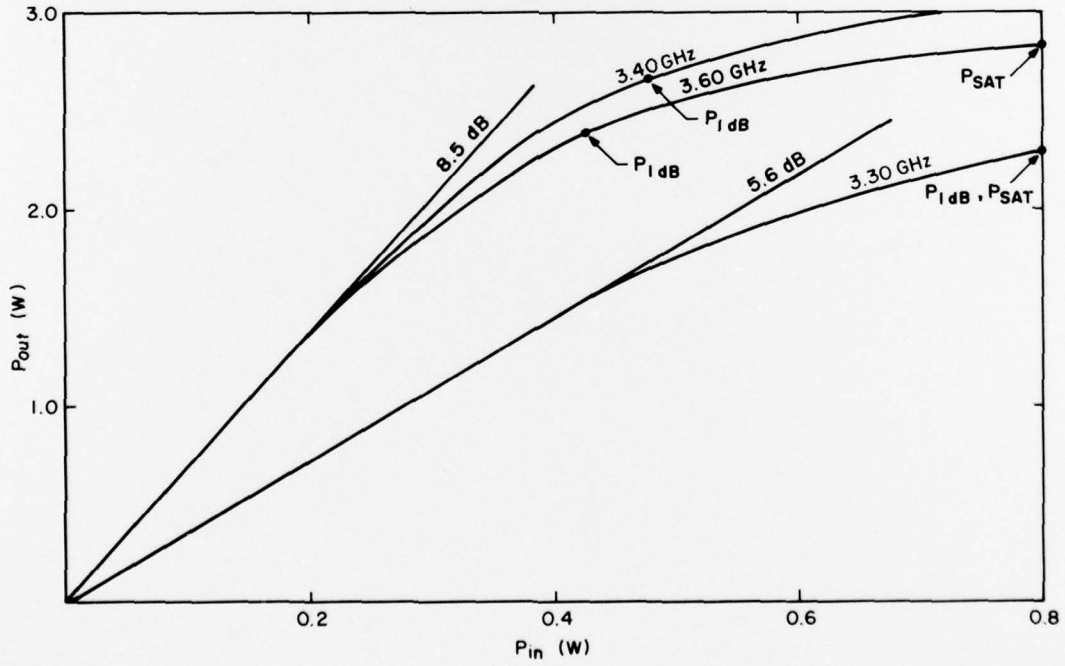

Figure 23. P_{out} vs P_{in} at 3.3, 3.4, and 3.6 GHz.

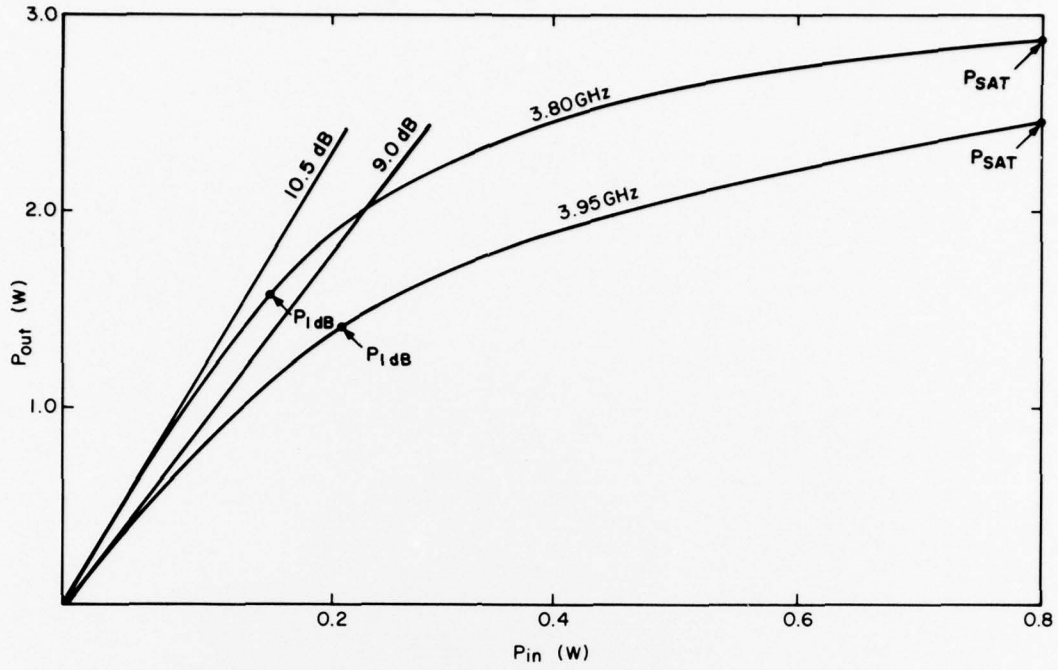

Figure 24. P_{out} vs P_{in} at 3.8 and 3.95 GHz.

Table 6. Single-Transistor Broadband Amplifier - Electrical Performances

Frequency (GHz)	Computed Gain (dB)	Measured Gain (dB)	$P_{1\,dB}$* (W)	P_{set}* (W)	$\eta_{1\,dB}$* (%)	η_{set}* (%)
3.4	7.2	8.5	2.70	3.05	12.8	13.0
3.6	8.6	8.5	2.45	2.85	11.5	11.8
3.8	11.3	10.5	1.60	2.90	8.2	12.1
3.95	10.0	9.0	1.35	2.45	6.6	9.5

*$P_{1\,dB}$ is the output power of 1-dB compression point;
P_{set} is the output power with P_{in} = 0.8 W; and
$\eta_{1\,dB}$, η_{set} are the efficiencies at the 1-dB point and at saturation defined as $(P_{out} - P_{in})/P_{\Delta c} \times 100$, respectively.

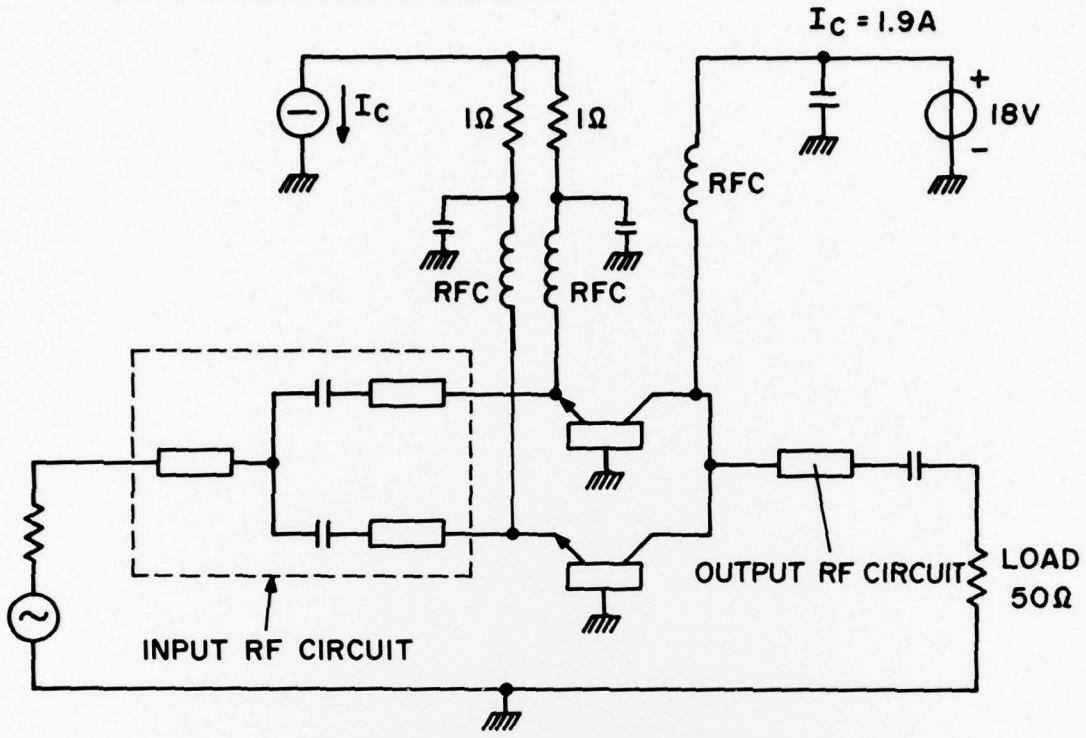

Figure 25. Dual-transistor amplifier - electrical schematic.

subsection III.B.3 above are shown in Fig. 26. It can be seen that the operating bandwidth is much narrower than that of the single-transistor amplifier, and the gain has a larger variation with frequency. Since the rf output power for a constant input power of 0.8 W follows, over frequency, the variation of the gain, we suspect the input matching circuit to be the cause of narrow bandwidth. This is supported by the fact that input impedance for the two transistors in parallel is very low, 1.5 ohms, and it is therefore difficult to match into it.

Best results were obtained at 3.7 GHz, which is also the resonant frequency of the shunt tuning. The rf output power of 5.8 W, obtained at this frequency, with 0.8-W input power represents a combining efficiency of about 90% when compared with the power obtainable from the transistors operated separately. The gain, at that same frequency, was also particularly high: 15 dB. The values of computed measured gain are listed in Table 7.

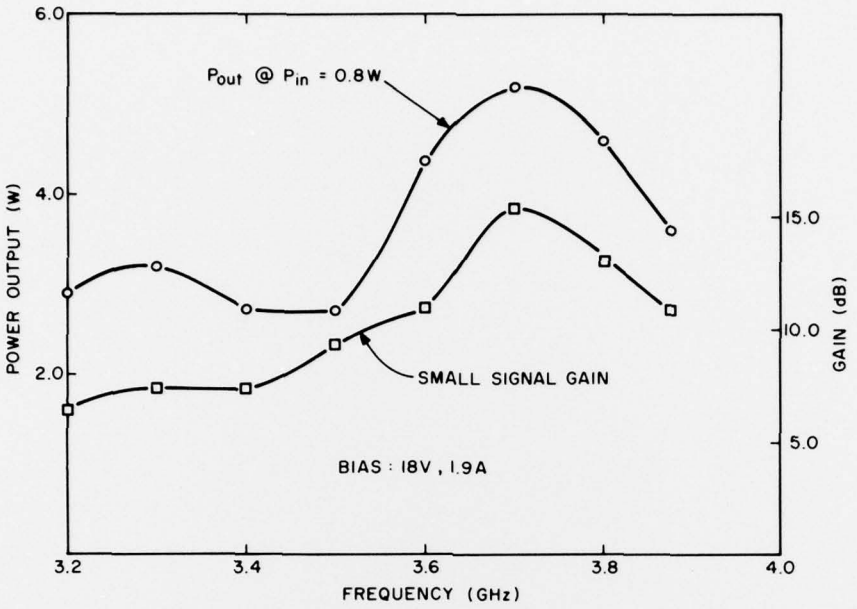

Figure 26. P_{out} and gain vs frequency - dual-transistor.

Table 7. Dual-Transistor Broadband Amplifier - Electrical Performances

Frequency (GHz)	Computed Gain (dB)	Measured Gain (dB)	P_{sat}* (W)	η_{sat}* (%)
3.20	-	6.4	4.2	7.6
3.30	-	7.4	4.1	7.3
3.40	5.6	7.4	3.3	4.9
3.50	6.4	9.3	3.3	4.9
3.60	7.4	10.9	4.5	8.4
3.70	10.0	15.4	5.3	10.8
3.80	11.3	13.0	5.1	10.2
3.87	10.0	10.9	4.4	8.1

Bias = 18 V, 1.9 A

*P_{sat} is the output power with P_{in} = 1.6 W and η_{sat} is the efficiency at saturation defined as $(P_{sat} - P_{in})/P_{\Delta c} \times 100$.

3. Construction

Both amplifiers have been constructed using transistors on BeO carriers described in subsection II.E. and microwave circuits built on 25-mil-thick AlO_2 ceramic substrates. Very low loss MOM capacitors were used in the microwave circuit as dc blocks and as rf bypasses on the "cold" sides of the rf chokes. Photographs of the two amplifiers are shown in Figs. 27 and 28. The overall dimensions of each amplifier are approximately 2.2 in. x 1.5 in. x 0.5 in.

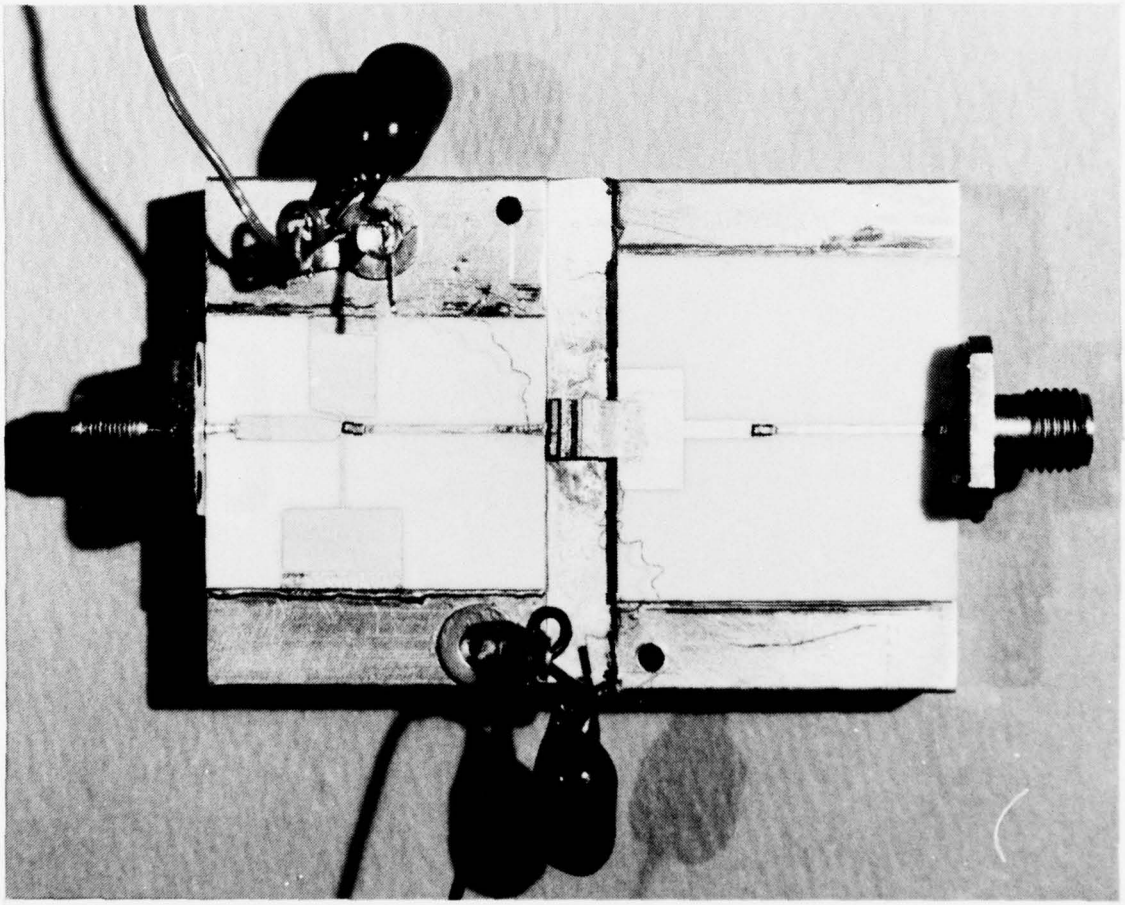

Figure 27. Photograph of single-transistor amplifier.

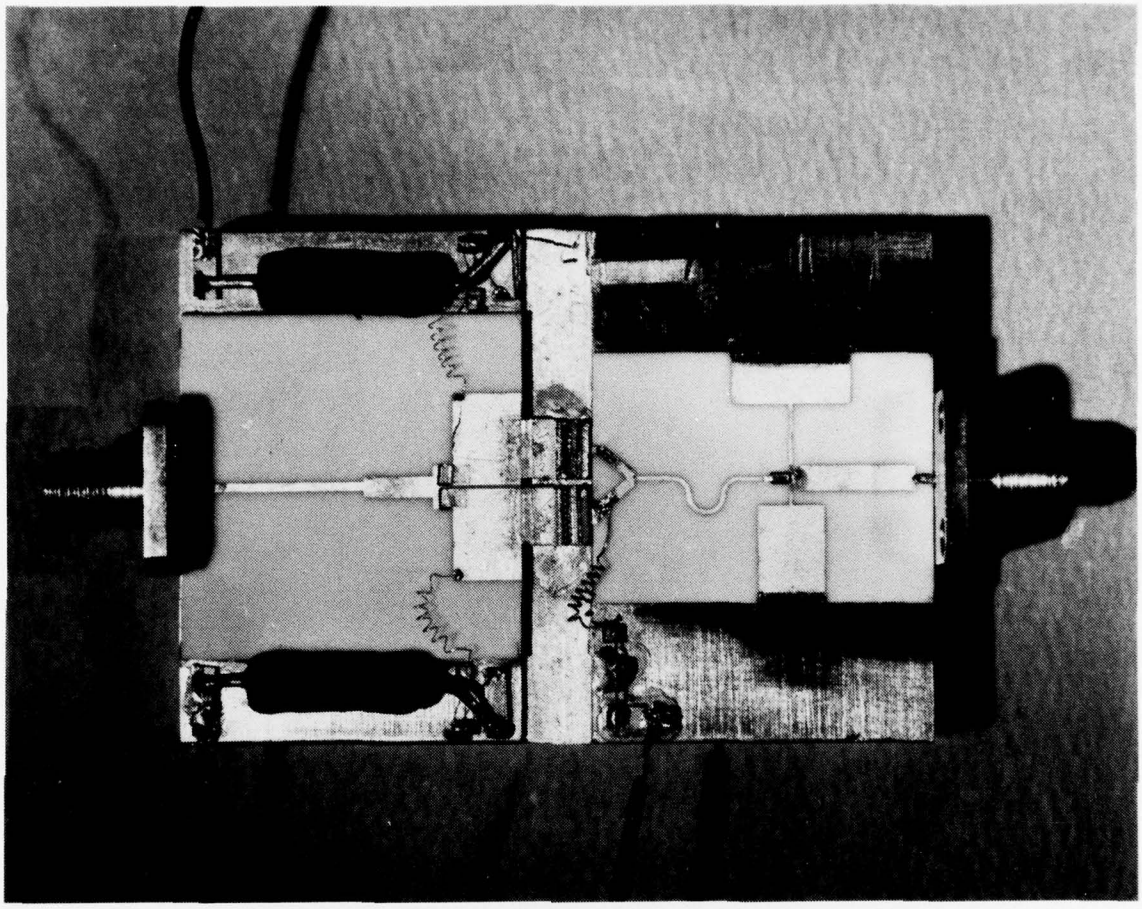

Figure 28. Photograph of dual-transistor amplifier.

SECTION IV

CONCLUSIONS

A high-power transistor, the RCA type TA8791, has been developed for operation in class A at 4 GHz. It can provide a minimum output power, at the 1-dB compression point, of 1.5 W up to a frequency of 4.0 GHz, with a small-signal gain of 13 dB and an efficiency of 9%. The output power is already 2.5 W at 3.6 GHz with an efficiency of 17% and rises to 4.0 W at 3.0 GHz with a corresponding efficiency of 24%. The performance achieved with the TA8791 is the result of several important improvements in the state-of-the-art of microwave power transistor processing.

The ion-implant process has been refined to allow the fabrication of transistors with good frequency and power performance. A number of experiments have been performed to optimize the doping levels and the annealing schedules.

The double-epitaxial layer has been found to be effective to reduce the rf losses in the collector without degradation of the base-collector voltage breakdown characteristics. Moreover, the metallurgical problems associated with the use of gold for the metallization pattern have been solved. The usefulness of this type of metallization stems from its high reliability and low rf losses.

A further improvement in performances has been obtained by thinning the silicon wafer to a 0.5-mil thickness and by plating a layer of copper about 3 mils thick in place of the removed silicon. This resulted in devices with excellent thermal characteristics and with very low rf losses in the collector region.

The above devices were used to build two broadband amplifiers, one utilizing a simple transistor and one utilizing two transistors paralleled directly in the microwave circuit. Best broadband performance was obtained with a single transistor amplifier which delivered 2.5 W of output power in the 3.4- to 3.8-GHz frequency range and a small-signal gain of 9 dB.

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